KXD9XXSB

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Shenzhen Kexinda Electronics Co., Ltd.

V1.2

Shenzhen Kexinda Electronics Co., Ltd.

Revised Apl 24, 2014

1 KXD9XXSB Overview

1.1 General Description

KXD9XXSB is a high-performance Controller for capacitive touch keys. Its engine is an 8-bit 80C52 compatible Processor.

KXD9XXSB has three timer/counters, maximum 24 channels of touch sensors, maximum 29 programmable I/O pins, 1 Sleep timer, 1 Watchdog timer, POR (Power-On Reset), UART, I^2C, and LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal ring oscillator, which can generate the 48 MHz system clock signal instead of a external oscillator.

KXD9XXSB has its own architecture for fast sensing. With the hardware filter, it provides noise immunity and excellent sensitivity. The firmware algorithm supports smart sensitivity and compensates for changes in the sensitivity due to environmental factors such as temperature and humidity.

To manage power effectively, KXD9XXSB enables low power consumption by using scan interval and clock control methods after last touch.

KXD9XXSB operates over the extended -20℃ to +85℃ temperature range, and is available in the 5mm x 5mm, 32-pin MLF/QFN or 24-pin MLF package.

1.2 Features

- Capacitive touch key controller
  - Supports up to 24 single-type touch keys
  - Supports scroll bar-type touch keys
  - Supports wheel-type touch keys
- Response Time
  - Programmable sensing rate for power saving.
- CPU
  - 8-bit Turbo 80C52 Architecture
  - 4 Cycles / 1 Machine Cycle

- Instruction Level Compatible with Intel 80C52

- Memory
  - 32kB Flash
  - 2KB Internal Aux. RAM
  - 256B Internal RAM
- Power Supply
  - Operating Voltage : +1.8V to +3.6V
- Operating Frequency: Max. 48MHz
- 29 Programmable I/O Pins
- Communication interfaces
  - 1-channel I2C Communication (Master/Slave)
  - 1-channel UART Communication
- Internal Ring OSC with Calibration function
- Supporting ISP/IAP/MDS
- 8 Internal Interrupt Sources and 4 External Interrupt Sources
- 4 Reset Sources
- Sleep (Power Down) Wake-up Sources
  - Reset Sources + 4 External Interrupt (Both Levels or Edge)
  - Sleep Timer wakeup event
  - WDT interrupt
- 4 Operating modes : Active, Idle, Sleep, Deep Seep(Halt)
  - Active : The CPU and all peripherals are ON.
  - Idle : The CPU is OFF and all or the part of peripherals can be ON.
    It can be woken up to Active mode by any interrupt sources.
  - Sleep : The CPU and all peripherals except sleep timer are OFF.
    The Sleep timer only is ON.
    It can be woken up to Active mode by sleep timer or external interrupts.
  - Deep Sleep(Halt) : The CPU and all peripherals including sleep timer are OFF.
    It can be woken up to Active mode by external interrupts only.
- E.S.D. Protection up to
  - 4,000V
- Latch-up Protection Up to ±200mA
- Package
  - 32-MLF (5mm X 5mm, 0.85T), 32-QFN (5mm X 5mm, 0.85T)
  - 24-MLF (4mm X 4mm, 0.85T)

1.3 Applications

- Home appliance: TV, Monitor, Home Theater, Remote Controller, etc.
- Mobile Phones
- Portable MP3, MP4
- Digital Cameras
- Navigation Systems & Automotive Applications
- Battery power applications

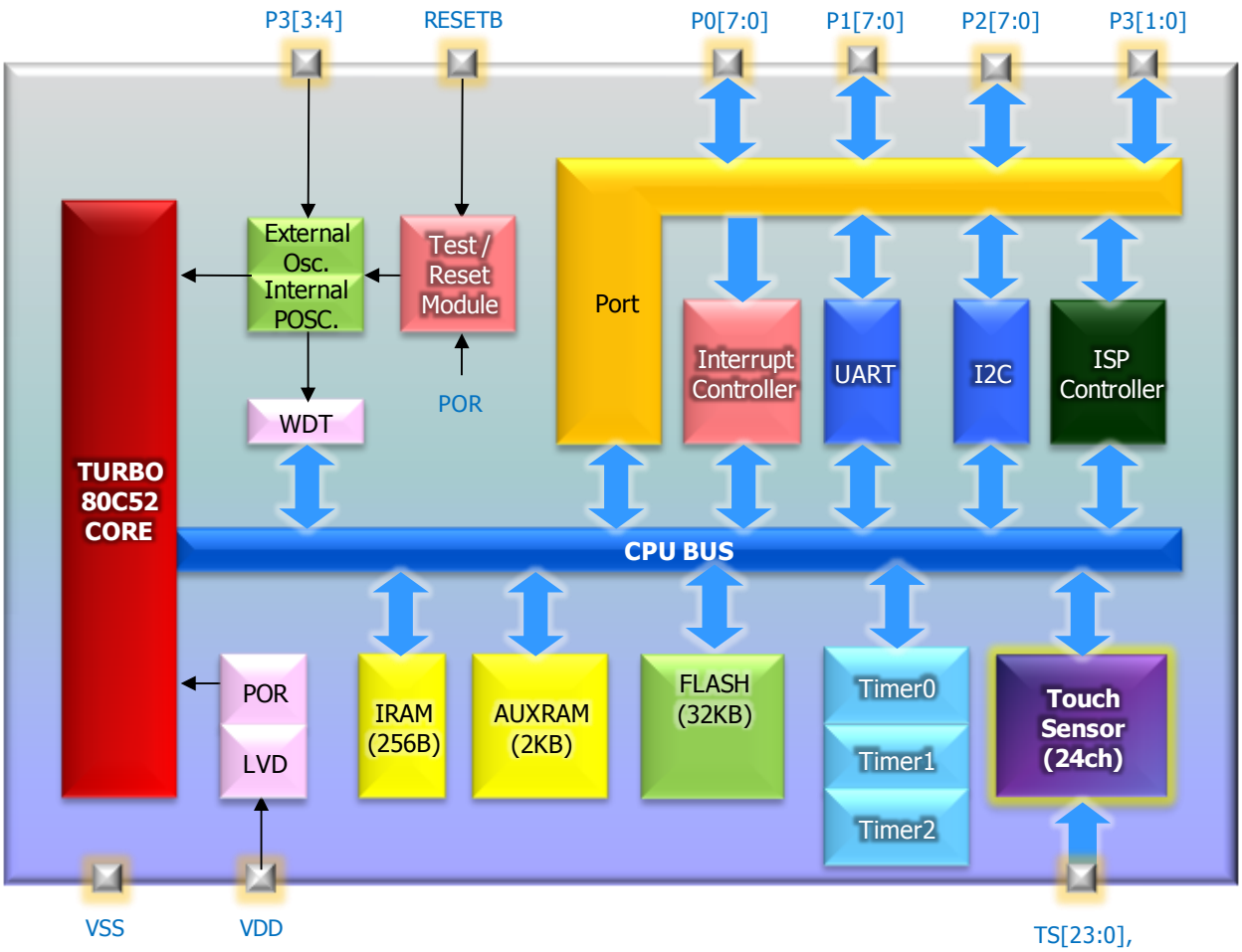
1.4 Product Family Guide

Product	FLASH, EEPROM [Byte]	RAM [Byte]	Volt [V]	T/C [16bits]	COM I/O	I/O Pins	Touch Channel,	Package	Others
KXD900SB-ML32IP	32k, (1k)	2k + 256	1.8 ~ 3.6	3	1 UART 1 I2C	27	23,	32-MLF (5X5X0.85)	IAP ISP EJTAG LVD POR RING
KXD910SB-QF32IP	32k, (1k)	2k + 256	1.8 ~ 3.6	3	1 UART 1 I2C	28	24,	32-QFN (5X5X0.85)	IAP ISP EJTAG LVD POR RING
KXD930SB-ML24IP	16k, (1k)	2k + 256	1.8 ~ 3.6	3	1 UART 1 I2C	19	16	24-MLF (4X4X0.85)	IAP ISP EJTAG LVD POR RING

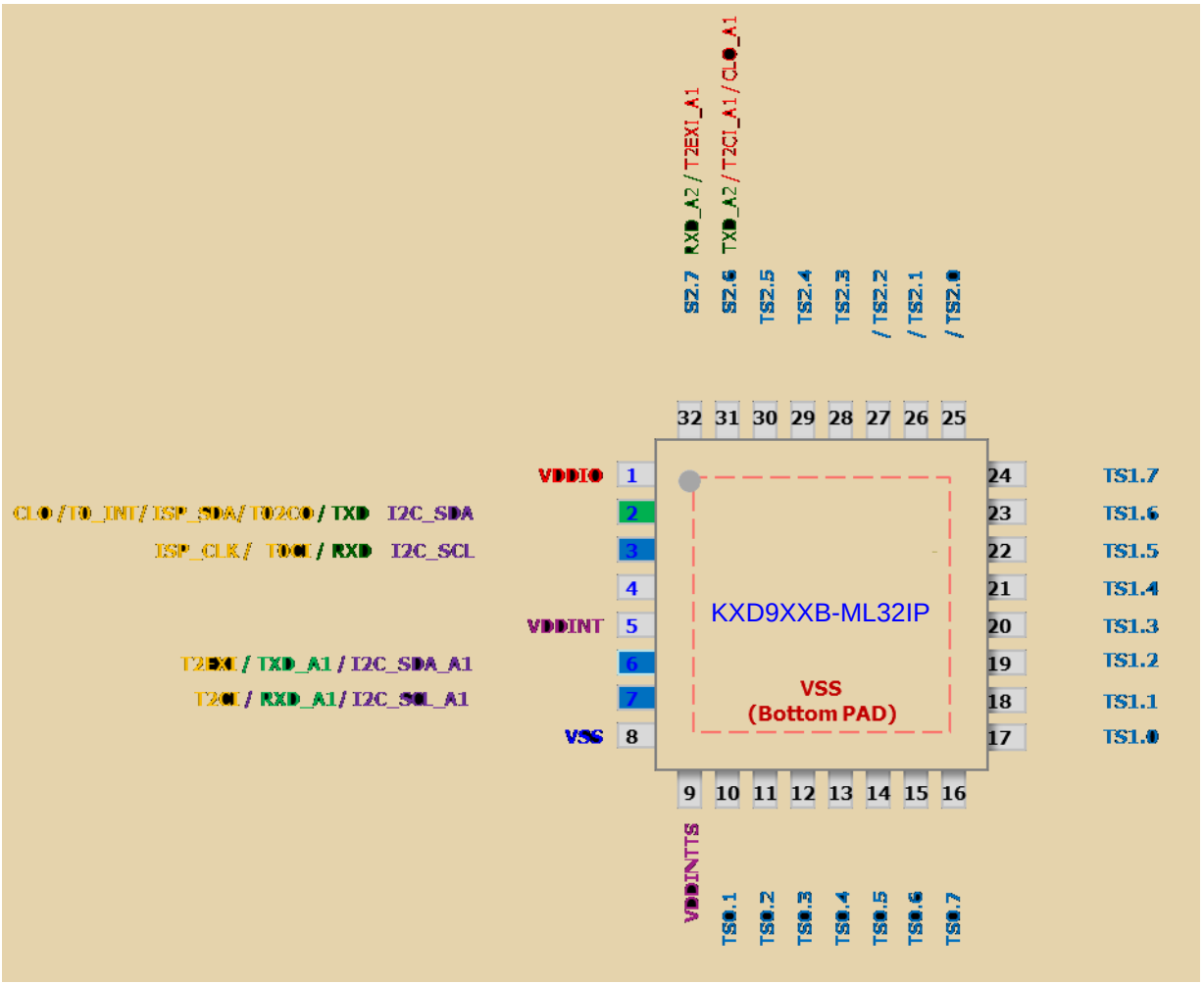
2 Block Diagram

Figure shows the block diagram of KXD9XXSB. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

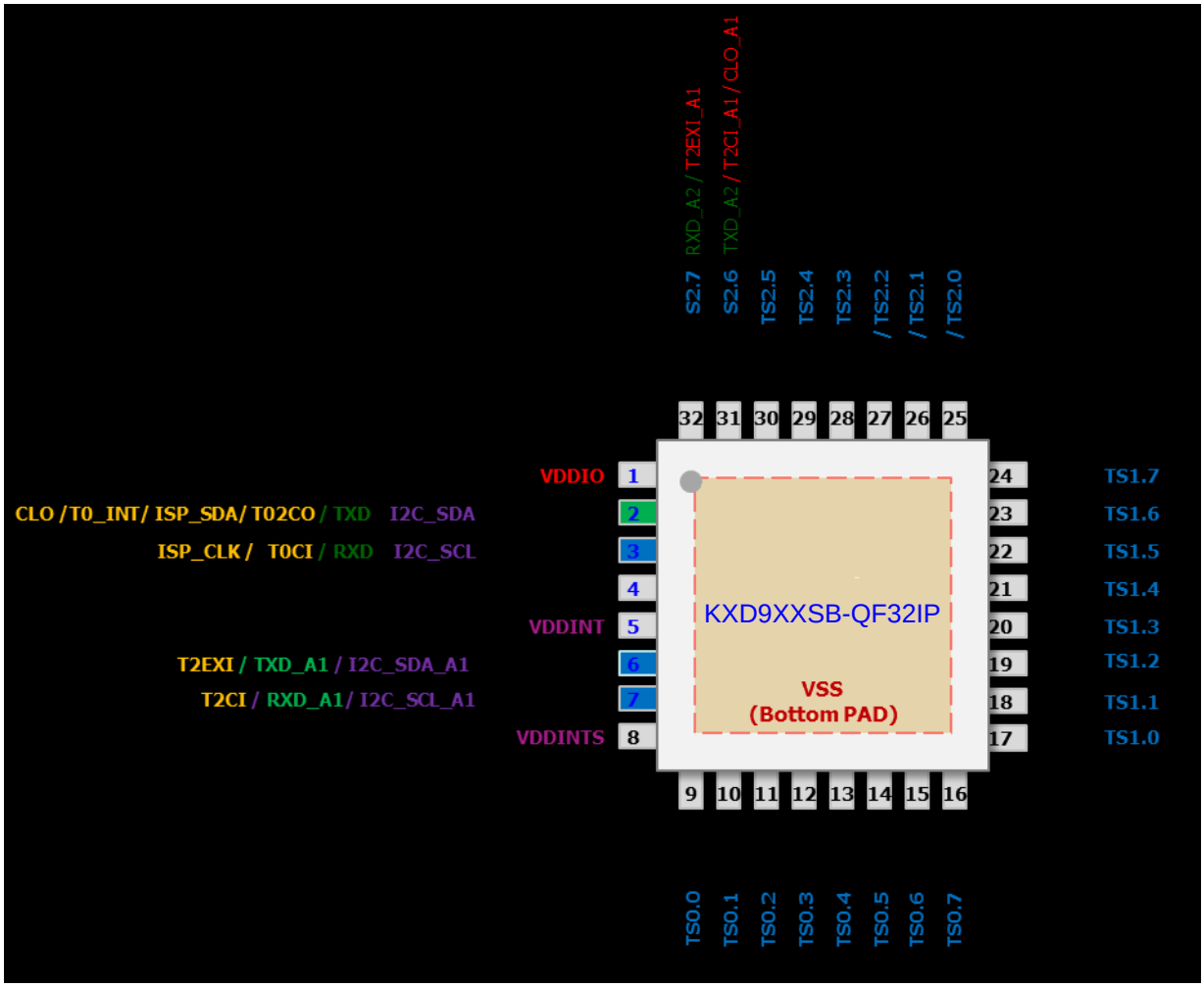
The internal registers of KXD9XXSB are configured as part of the on-chip RAM: therefore each register has an address. This is reasonable for KXD9XXSB, since it has so many registers.



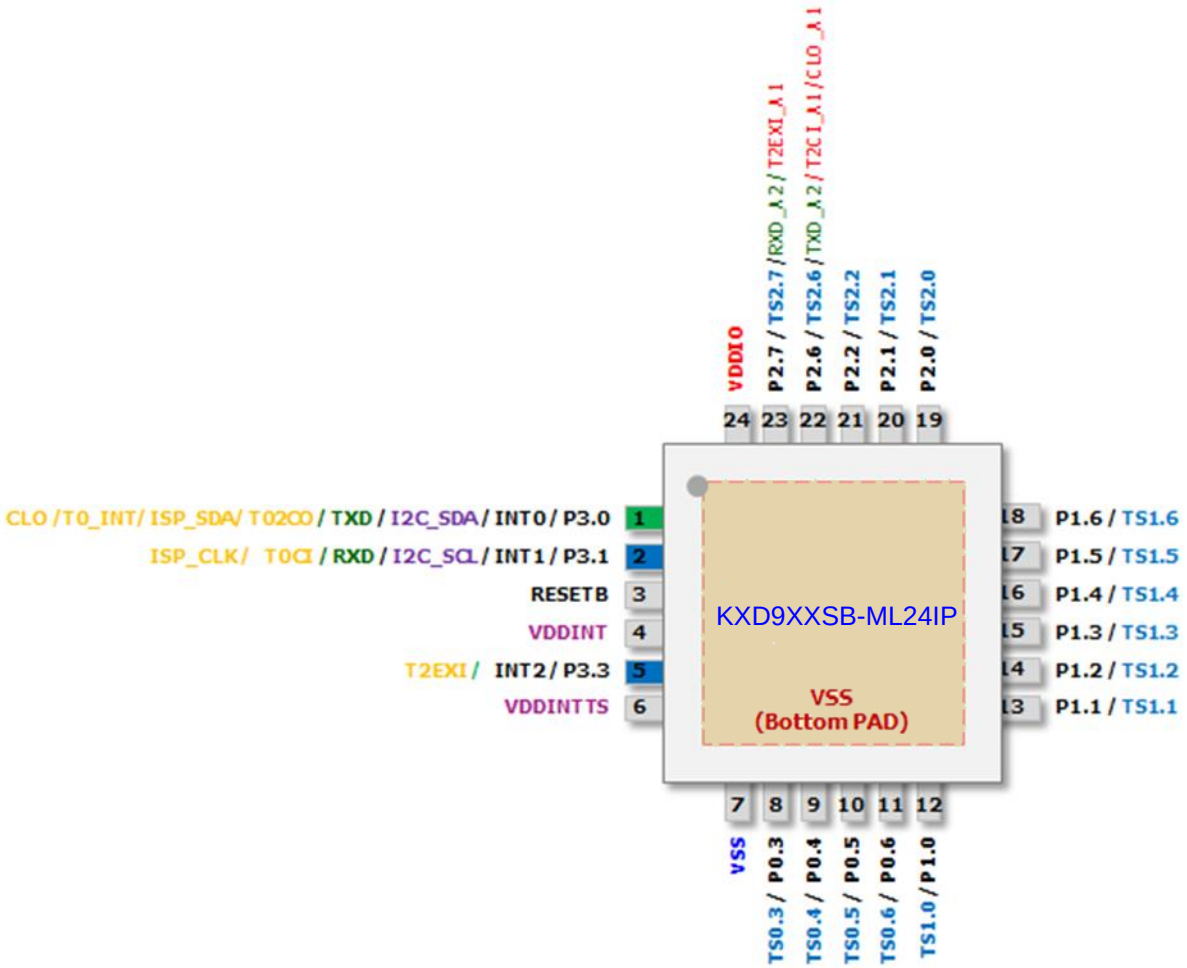
3 Pin Configuration



32-pin MLF Package Diagram



32-pin QFN Package Diagram



24-pin MLF Package Diagram

4 Pin Description

32-pin MLF

Pin No.	Name	Type	Description	Share Pins
1	VDDIO	PWR	Power	
2	P3.0	I/O	General I/O Port 3.0	T0_INT / T02CO / TXD / I2C1_SDA / INT0
3	P3.1	I/O	General I/O Port 3.1	T0CI / RXD / I2C1_SCL / INT1
4	RESETB	I	Reset Input	
5	VDDINT	O	Digital Power Filter (+1.8V)	
6	P3.3	I/O	General I/O Port 3.3	T2EXI / TXD_A/ I2C1_SDA_A / XTAL2 / INT3
7	P3.4	I/O	General I/O Port 3.4	T2CI / RXD_A /I2C1_SCL_A / XTAL1 / INT4
8	VSS	GND	Gound	
9	VDDINTS	O	Touch Power Filter	
10	TS0.1	I/O	Touch Sensing Channel 0.1	P0.1
11	TS0.2	I/O	Touch Sensing Channel 0.2	P0.2
12	TS0.3	I/O	Touch Sensing Channel 0.3	P0.3
13	TS0.4	I/O	Touch Sensing Channel 0.4	P0.4
14	TS0.5	I/O	Touch Sensing Channel 0.5	P0.5
15	TS0.6	I/O	Touch Sensing Channel 0.6	P0.6
16	TS0.7	I/O	Touch Sensing Channel 0.7	P0.7
17	TS1.0	I/O	Touch Sensing Channel 1.0	P1.0
18	TS1.1	I/O	Touch Sensing Channel 1.1	P1.1
19	TS1.2	I/O	Touch Sensing Channel 1.2	P1.2
20	TS1.3	I/O	Touch Sensing Channel 1.3	P1.3
21	TS1.4	I/O	Touch Sensing Channel 1.4	P1.4
22	TS1.5	I/O	Touch Sensing Channel 1.5	P1.5
23	TS1.6	I/O	Touch Sensing Channel 1.6	P1.6
24	TS1.7	I/O	Touch Sensing Channel 1.7	P1.7
25	TS2.0	I/O	Touch Sensing Channel 2.0	P2.0
26	TS2.1	I/O	Touch Sensing Channel 2.1	P2.1
27	TS2.2	I/O	Touch Sensing Channel 2.2	P2.2
28	TS2.3	I/O	Touch Sensing Channel 2.3	P2.3
29	TS2.4	I/O	Touch Sensing Channel 2.4	P2.4
30	TS2.5	I/O	Touch Sensing Channel 2.5	P2.5
31	TS2.6	I/O	Touch Sensing Channel 2.6	P2.6_A2 / T2CI_A1 / CLO_A1
32	TS2.7	I/O	Touch Sensing Channel 2.7	P2.7 / RXD_A2 / T2EXI_A1

32-pin QFN

Pin No.	Name	Type	Description	Share Pins
1	VDDIO	PWR	Power	
2	P3.0	I/O	General I/O Port 3.0	T0_INT / T02CO / TXD / I2C1_SDA / INT0
3	P3.1	I/O	General I/O Port 3.1	T0CI / RXD / I2C1_SCL / INT1
4	RESETB	I	Reset Input	
5	VDDINT	O	Digital Power Filter (+1.8V)	
6	P3.3	I/O	General I/O Port 3.3	T2EXI / TXD_A/ I2C1_SDA_A / XTAL2 / INT3
7	P3.4	I/O	General I/O Port 3.4	T2CI / RXD_A /I2C1_SCL_A / XTAL1 / INT4
8	VDDINTS	O	Touch Power Filter	
9	TS0.0	I/O	Touch Sensing Channel 0.0	P0.0
10	TS0.1	I/O	Touch Sensing Channel 0.1	P0.1
11	TS0.2	I/O	Touch Sensing Channel 0.2	P0.2
12	TS0.3	I/O	Touch Sensing Channel 0.3	P0.3
13	TS0.4	I/O	Touch Sensing Channel 0.4	P0.4
14	TS0.5	I/O	Touch Sensing Channel 0.5	P0.5
15	TS0.6	I/O	Touch Sensing Channel 0.6	P0.6
16	TS0.7	I/O	Touch Sensing Channel 0.7	P0.7
17	TS1.0	I/O	Touch Sensing Channel 1.0	P1.0
18	TS1.1	I/O	Touch Sensing Channel 1.1	P1.1
19	TS1.2	I/O	Touch Sensing Channel 1.2	P1.2
20	TS1.3	I/O	Touch Sensing Channel 1.3	P1.3
21	TS1.4	I/O	Touch Sensing Channel 1.4	P1.4
22	TS1.5	I/O	Touch Sensing Channel 1.5	P1.5
23	TS1.6	I/O	Touch Sensing Channel 1.6	P1.6
24	TS1.7	I/O	Touch Sensing Channel 1.7	P1.7
25	TS2.0	I/O	Touch Sensing Channel 2.0	P2.0
26	TS2.1	I/O	Touch Sensing Channel 2.1	P2.1
27	TS2.2	I/O	Touch Sensing Channel 2.2	P2.2
28	TS2.3	I/O	Touch Sensing Channel 2.3	P2.3
29	TS2.4	I/O	Touch Sensing Channel 2.4	P2.4
30	TS2.5	I/O	Touch Sensing Channel 2.5	P2.5
31	TS2.6	I/O	Touch Sensing Channel 2.6	P2.6 / TXD_A2 / T2CI_A1 / CLO_A1
32	TS2.7	I/O	Touch Sensing Channel 2.7	P2.7 / RXD_A2 / T2EXI_A1

24-pin MLF

Pin No.	Name	Type	Description	Share Pins
1	P3.0	I/O	General I/O Port 3.0	T0_INT / T02CO / TXD / I2C1_SDA / INT0
2	P3.1	I/O	General I/O Port 3.1	T0CI / RXD / I2C1_SCL / INT1
3	RESETB	I	Reset Input	
4	VDDINT	O	Digital Power Filter (+1.8V)	
5	P3.3	I/O	General I/O Port 3.3	T2EXI / TXD_A/ I2C1_SDA_A / XTAL2 / INT3
6	VDDINTS	O	Touch Power Filter	
7	VSS	GND	Gound	
8	TS0.3	I/O	Touch Sensing Channel 0.3	P0.3
9	TS0.4	I/O	Touch Sensing Channel 0.4	P0.4
10	TS0.5	I/O	Touch Sensing Channel 0.5	P0.5
11	TS0.6	I/O	Touch Sensing Channel 0.6	P0.6
12	TS1.0	I/O	Touch Sensing Channel 1.0	P1.0
13	TS1.1	I/O	Touch Sensing Channel 1.1	P1.1
14	TS1.2	I/O	Touch Sensing Channel 1.2	P1.2
15	TS1.3	I/O	Touch Sensing Channel 1.3	P1.3
16	TS1.4	I/O	Touch Sensing Channel 1.4	P1.4
17	TS1.5	I/O	Touch Sensing Channel 1.5	P1.5
18	TS1.6	I/O	Touch Sensing Channel 1.6	P1.6
19	TS2.0	I/O	Touch Sensing Channel 2.0	P2.0
20	TS2.1	I/O	Touch Sensing Channel 2.1	P2.1
21	TS2.2	I/O	Touch Sensing Channel 2.2	P2.2
22	TS2.6	I/O	Touch Sensing Channel 2.6	P2.6_A2 / T2CI_A1 / CLO_A1
23	TS2.7	I/O	Touch Sensing Channel 2.7	P2.7 / RXD_A2 / T2EXI_A1
24	VDDIO	PWR	Power	

5 Absolute Maximum Ratings

Absolute Maximum Ratings(TA = 25 °C)

Item	Conditions	Range
DC Voltage in V_{DDIO} relative to Ground	-	-0.5 V to +3.6V
DC Input Voltage	-	-0.5V to (V_{DDIO}+0.5V)
DC Output Voltage	-	-0.5 V to (V_{DDIO}+0.5V)
DC Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
DC Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Storage Temperature	-	-65 °C to +150 °C
Soldering Temperature	-	260 °C for 10 seconds

Recommended Operating Conditions

Item	Conditions	Range
Operating Voltage	-	+1.8 V to +3.6V
DC Input Voltage	-	-20℃ to + 85℃

6 DC Characteristics

6.1 I/O Port Pin Characteristics

* T_A= -20°C ~ +85°C, V_{DD}=1.8V ~ 3.6V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL}	P0,P1,P2,P3	V_{DDIO} = 1.8V~3.6V	-0.5	-	$0.2V_{DDIO}$+0.1	V
Input high Voltage	V_{IH}	P0,P1,P2,P3	V_{DDIO} = 1.8V~3.6V	$0.2V_{DDIO}$+1.0	-	V_{DDIO}+0.5	V
Output Low Voltage	V_{OL}	P0,P1,P2,P3	V_{DDIO} = 3.3V (I_{OL} = 7.69mA) V_{DDIO} = 1.8V (I_{OL} = 2.24mA)	-	-	$0.3V_{DDIO}$	V
		P0,P1,P2,P3 (High Drive)	V_{DDIO} =3.3V (I_{OL} = 61.51mA) V_{DDIO} = 1.8V (I_{OL} = 17.88mA)	-	-	$0.3V_{DDIO}$	V
Output High Voltage	V_{OH}	P0,P1,P2,P3	V_{DDIO} = 3.3V (I_{OL} = -12.12mA) V_{DDIO} = 1.8V (I_{OL} = -3.88mA)	$0.7V_{DDIO}$	-	-	V
	V_{OH}	P0,P1,P2,P3 (High Drive)	V_{DDIO} = 3.3V (I_{OL} = -96.93mA) V_{DDIO} = 1.8V (I_{OL} = -32.07mA)	$0.7V_{DDIO}$	-	-	V
	V_{OHP}	P0,P1,P2,P3 (Pull-up Resistor Only), Except P3[4:3,1]	V_{DDIO} = 3.0V~3.6V (I_{OL} = -47.85uA) V_{DDIO} = 1.8V~3.0V (I_{OL} = -12.73uA)	$0.7V_{DDIO}$	-	-	V
Input Leakage Current	I_{IL}	P0,P1,P2,P3	V_{IN} = V_{IH} or V_{IL}	-	-	±1	μA
Pull-up Resistor	R_{pu}	All pins Except P3[4:3,1]	V_{DDIO}=+3.3V		52		KΩ
Pin Capacitance	C_{IO}	All	V_{DDIO} = 3.0V	-	10	-	pF

6.2 Current Characteristics

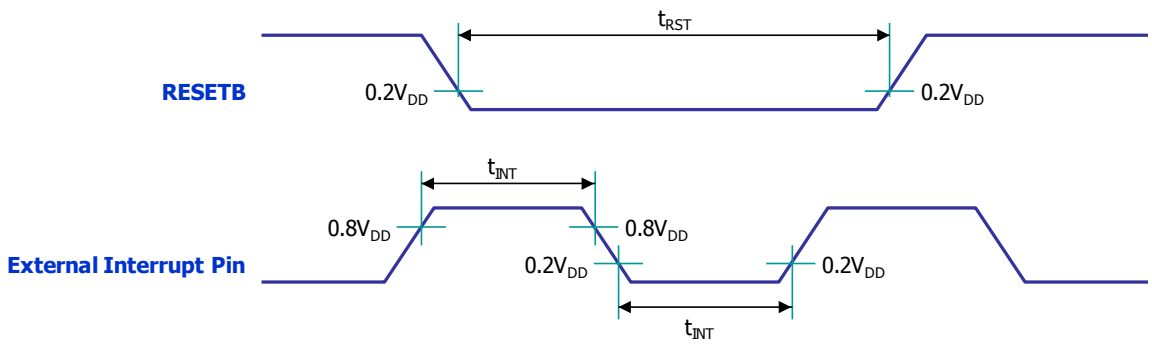
* T_A = -20°C ~ +85 °C , unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Current in Active Mode	IDD_{active}	CPU=48MHz, V_{DDIO}= 3.3V		2.7		mA
Current in Sleep Mode	IDD_{sleep1}	V_{DDIO} = 3.3V		36		uA
Current in Deep Sleep mode	IDD_{sleep2}	V_{DDIO} = 3.3V		6		uA

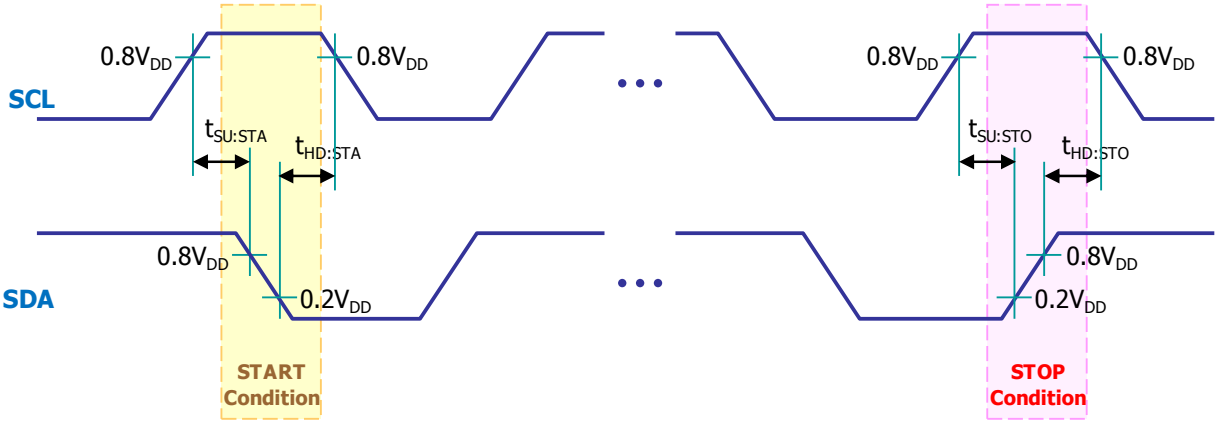
7 AC Characteristics

* T_A = -20°C ~ +85 °C, V_{DD} = 1.8V ~ 3.6V unless otherwise specified

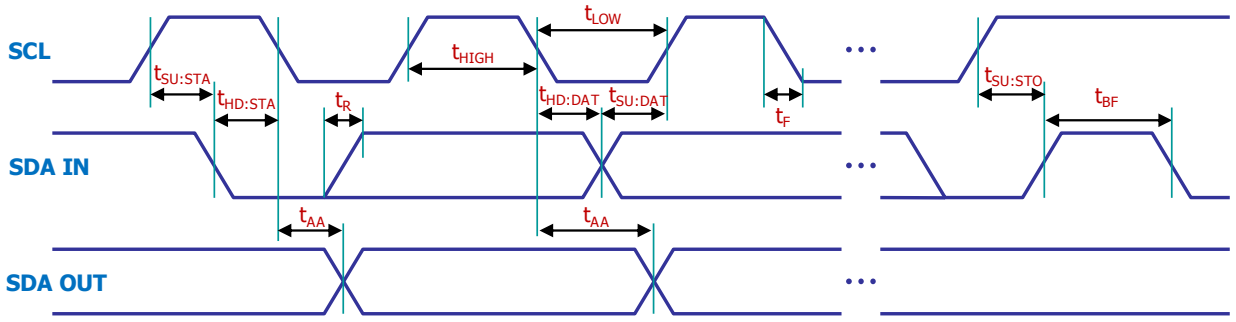
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
RESETB Input Width	t_{RST}	RESETB	V_{DD} = 3V ± 10% V_{DD} = 1.8V ± 10%	64	-	-	F_{SYS}
External Interrupt Input Width	t_{INT}	External Interrupt	V_{DD} = 3V ± 10% V_{DD} = 1.8V ± 10%	4	-	-	F_{SYS}



8 I2C Timing Characteristics

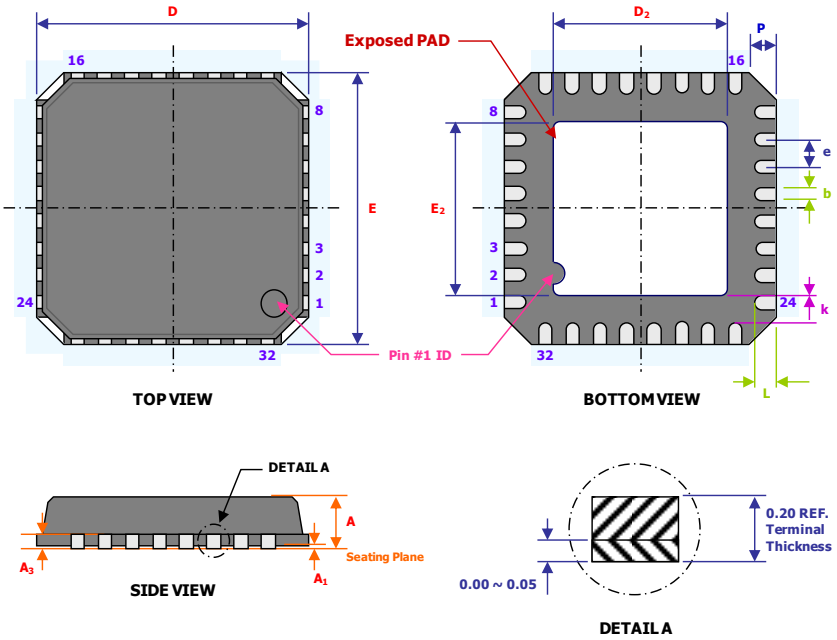


Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
$t_{SU:STA}$	START Condition Setup Time	100kHz Mode	4,700	-	Only relevant for repeated START condition
		400kHz Mode	600	-	
$t_{HD:STA}$	START Condition Hold Time	100kHz Mode	4,700	-	After this period, the first clock pulse is generated
		400kHz Mode	600	-	
$t_{SU:STO}$	STOP Condition Setup Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	
$t_{HD:STO}$	STOP Condition Hold Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	



Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
t_{HIGH}	Clock High Time	100kHz Mode	4,000	-	Minimum Frequency : 2MHz
		400kHz Mode	600	-	Minimum Frequency : 4MHz
t_{LOW}	Clock Low Time	100kHz Mode	4,700	-	Minimum Frequency : 2MHz
		400kHz Mode	1,300	-	Minimum Frequency : 4MHz
$t_{SU:DAT}$	Data Input Setup Time	100kHz Mode	250	-	
		400kHz Mode	100	-	
$t_{HD:DAT}$	Data Input Hold Time	100kHz Mode	0	-	
		400kHz Mode	0	900	
t_{AA}	Data Valid from Clock	100kHz Mode	-	3,500	
		400kHz Mode	-	-	
t_{BF}	BUS Free Time	100kHz Mode	4,700	-	
		400kHz Mode	1,300	-	
t_R	SDA & SCL Rising Time	100kHz Mode	-	1,000	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	
t_F	SDA & SCL Falling Time	100kHz Mode	-	300	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	

9 32-pin MLF Package Dimension

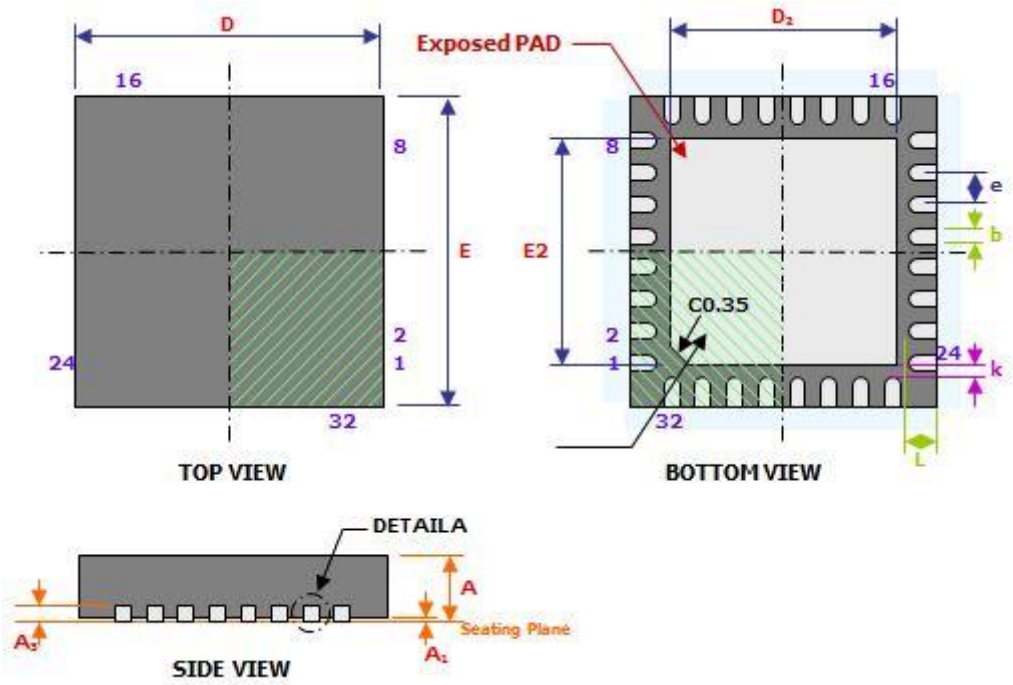


Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.01	0.05
A_3		0.20 REF	
D		5.00 BSC	
E		5.00 BSC	
D_2	2.60	2.70	2.80
E_2	2.60	2.70	2.80
b	0.18	0.23	0.30
e		0.50 BSC	
L	0.30	0.40	0.50
k	0.20	-	-
P	0.24	0.42	0.60

Notes:

1. All Dimension are in mm. Angles in Degrees.
2. Dimension b applies to Plated Terminal & is measured.
3. BSC : Basic Dimension. Theoretically exact value shown without tolerances.
   REF : Reference Dimension, Usually without tolerance, for information purpose only

10 32-pin QFN Package Dimension

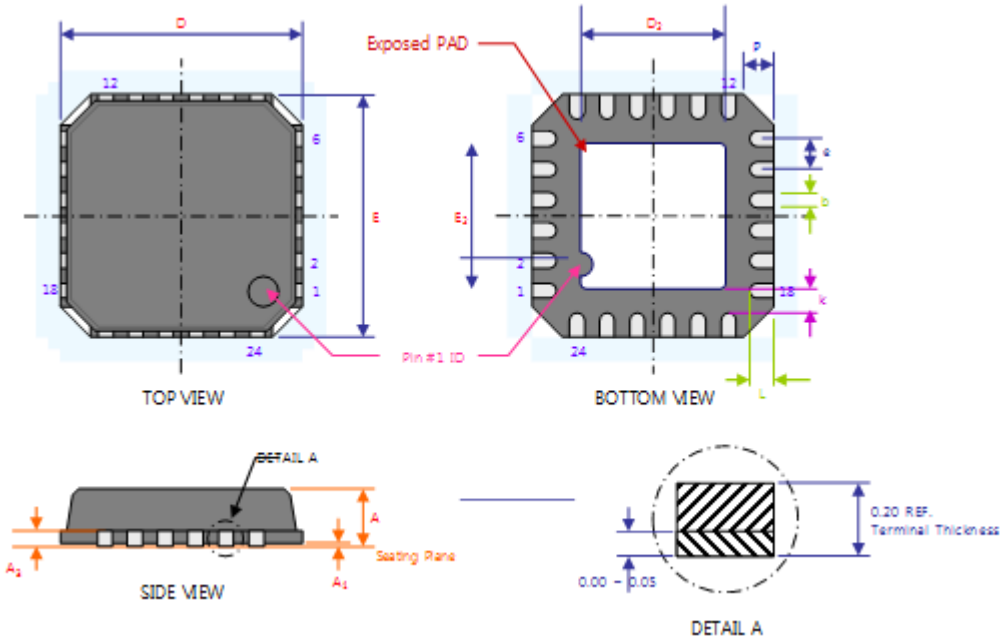


Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.02	0.05
A_3	0.20 REF		
D	5.00 BSC		
E	5.00 BSC		
D_2	3.50	3.60	3.70
E_2	3.50	3.60	3.70
b	0.18	0.25	0.30
e	0.50 BSC		
L	0.35	0.40	0.45
k	0.20	-	-

Notes:

1. All Dimension are in mm. Angles in Degrees.
2. Dimension b applies to Plated Terminal & is measured.
3. BSC : Basic Dimension. Theoretically exact value shown without tolerances.
   REF : Reference Dimension, Usually without tolerance, for information purpose only

11 24-pin MLF Package Dimension



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.01	0.05
A_3	0.20 REF		
D	4.00 BSC		
E	4.00 BSC		
D_2	2.40	2.50	2.60
E_2	2.40	2.50	2.60
b	0.18	0.23	0.30
e	0.50 BSC		
L	0.30	0.40	0.50
k	0.20	-	-
P	0.24	0.42	0.60

Notes:

1. All Dimension are in mm. Angles in Degrees.
2. Dimension b applies to Plated Terminal & is measured.
3. BSC : Basic Dimension. Theoretically exact value shown without tolerances.
   REF : Reference Dimension, Usually without tolerance, for information purpose only

12 Revision History

Date	Revision	History
February-2014	1.0	Initial Release of Document (KXD9XXSBversion SPEC)
April-2014	1.1	KXD930SB Update
April-2014	1.2	KXD930SB Update