Preliminary

TTU010 / TTR010 (IR remote 1K MCU)

§ General Description:

TTU10/TTR010 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1K-word ROM、48-nibble RAM、timer/Counter、interrupt service 、IO control hardware、carrier generation timer which is especially designed for infrared remote appliance.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 24 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1K*16 program ROM and 48*4 SRAM
6. 1-level stacks
7. Operating voltage: 1.8V~3.6V for resonator oscillator (400KHz~4MHz)
8. System operating frequency: (at VDD=3V)
   . High speed system oscillator (OSCH):
   - ✧ Resonator mode: 400KHz~4MHz for SR010/SU010

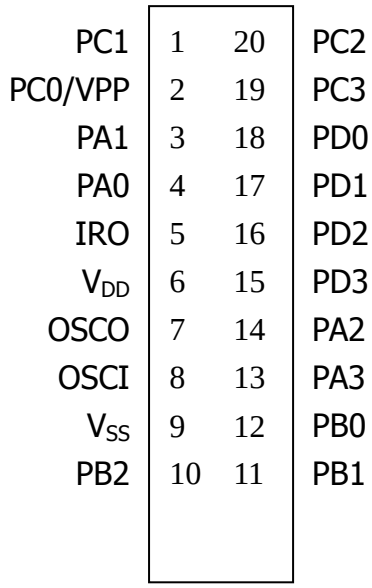
   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical)
9. Offers 18 general open drain I/O or input pins
   - ✧ 8 input port with wakeup function
   - ✧ 8 open drain IO port
   - ✧ 2 open drain IO port with CMOS/NMOS output option
   - ✧ Offering typical 350mA output driver directly drive IR LED
10. Two 8-bit auto-reload timer/counter
    - ✧ One special timer for carrier generation(duty & frequency)
    - ✧ One standard timer offers interrupt request
11. MCU system protection:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ Low voltage Reset(LVR)
12. Provides 2 interrupt sources
    - ✧ Internal: Timer/counter A & B

13. Provide package types
    - ✧ DIP/SOP/SSOP 16/20/24 pins
    - ✧ Dice available

§ Applications:

1. Infrared remote control transmitter
2. AV & household electrical appliance
3. Serial programming retail remote control

§ Package type:



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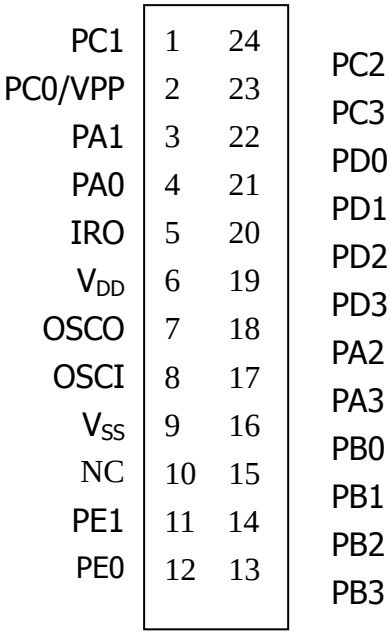

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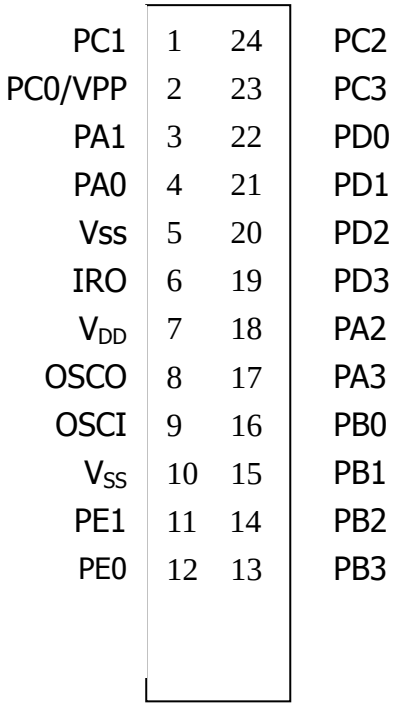

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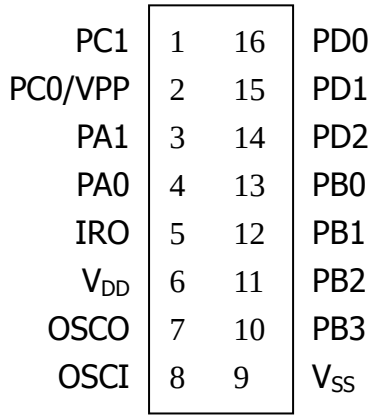
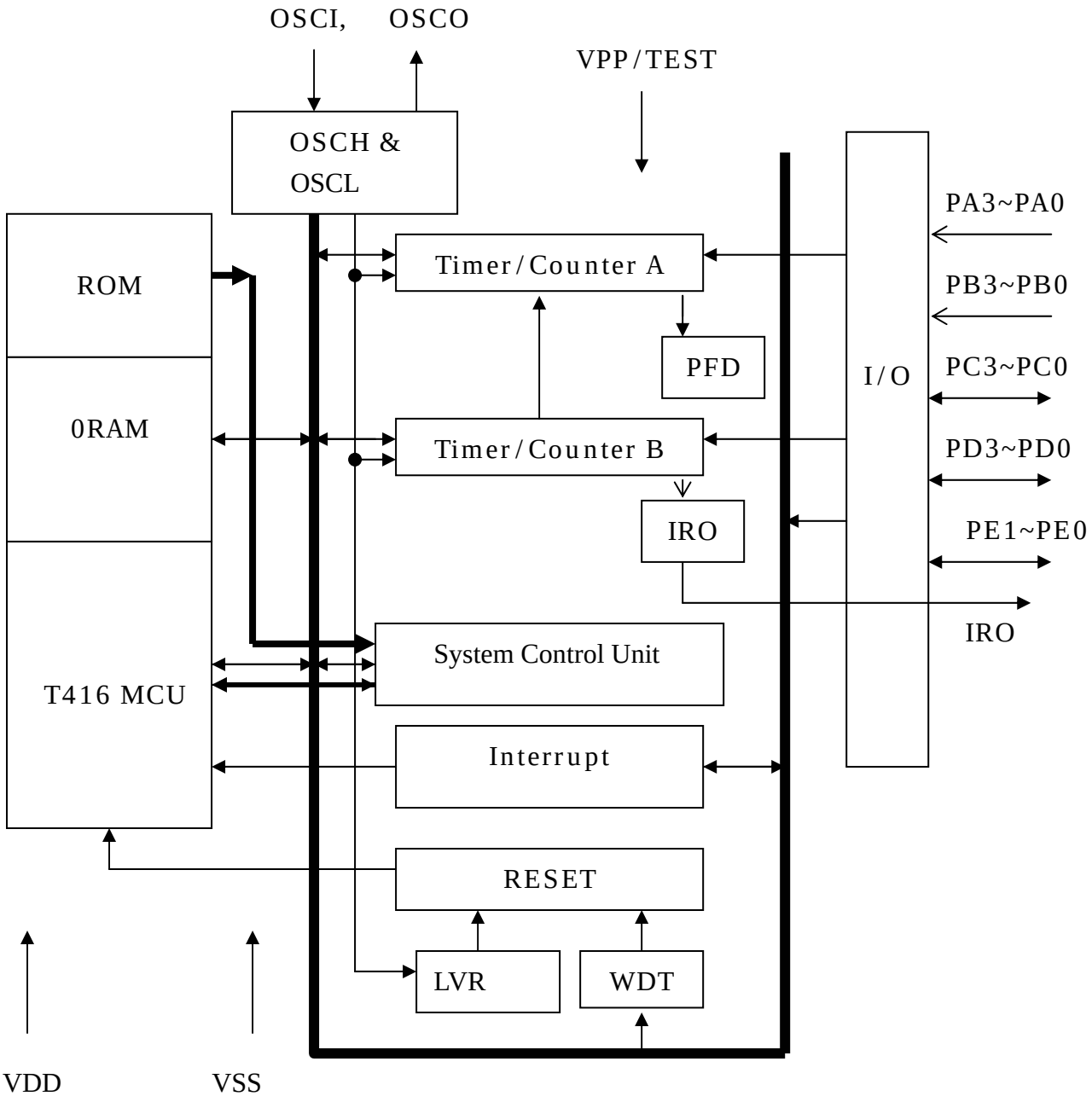


16-SOP-A

§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
PA0~PA3		I	+4		Input port PA
V_{SS}		Power	+1		Negative power supply, ground
IRO		O	+1	IROIROB	IRO output
V_{DD}		Power	+1		Positive power supply
OSCI OSCO		I O	+1 +1		Crystal/resonator oscillator terminals
V_{SS}		Power	+1		Negative power supply, ground
PD0		IO	+1		Open drain type IO port
PE0~PE1		IO	+2		Open drain type IO port
PD1~PD3		IO	+3		Open drain type IO port
PC0 PC1~PC3		IO IO	+1 +4		PC0 shares pad with VPP pin Open drain type IO port
PB0~PB3		I	+4		Input port

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA3,PB0~PB3	Figure IO-E	Input Port
PC0~PC3,PD0~PD3, PE0~PE1	Figure IO-F	STD open drain IO Port
IRO	Figure IO-G	STD Output Port

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20°C ~ +70°C	°C
Storage Temperature	Tst	-50°C ~ +125°C	°C
Supply Voltage	VDD	VSS-0.3 ~VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 to VDD+0.3	V
Human Body Mode	ESD	>3	KV
Note: VSS symbolizes for system ground			

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	Resonator/Crystal F_{OSCH}=400K~4MHz	**1.8**	-	3.6	V
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd1}	VDD=3.0V, no load, F_{OSCH}=2MHz,	-	1.0	2.0	mA
	I_{nd3}	VDD=3.0V, no load, F_{OSCH}=455KHz,		0.4	0.7	
Standby Current	Istb	I/O no load, F_{OSCH} & F_{OSCL} stop	-	-	1.0	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
PC,PD Sink Current	I_{OL1}	VDD=3.0V, Vol=0.6V	2	4	-	mA
IRO Sink Current	I_{OL2}	V_{DD}=3V, V_{OL}=0.6V	300	350	-	mA
PD2,PD3 output source current	I_{OH}	VDD=3.0V, Voh=-0.0V	10	-	30	uA
PA,PB pull-high Resistor	R_{PH}	VDD=3.0V	50	100	150	KΩ
Oscillator Start up voltage	$\mathbf{V_{ST}}$	F_{OSC}=455k~2M	1.8	-	2.0	V
Oscillator Sustain voltage	$\mathbf{V_{SU}}$	F_{OSC}=455K~2M	1.3	-	1.5	V

§ AC Characteristics:

Parameter	Test Condition		Min	Typ.	Max	Unit
Wake up input	Low active pulse width t_{wkup}, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH}(Crystal)	VDD=3.0V	400K	-	4M	Hz
Startup Period of Oscillators	T_{OSCH} (Crystal)	wake-up from off mode	-	4	-	F_{OSCH}
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		32	35	40	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$3FF_H$		Program ROM [1K*16]
	000_H ~ 007_H	File Registers
	008_H~$01F_H$	Peripheral registers (I)
	020_H~$04F_H$	Working RAM [48*4]

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESETB
$001	Hardware IRQB /Soft IRQB

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers: Interrupt request flag register

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	0100	CPU power saving control register
009_H	INTC	R/W	0000	Interrupt enable control register
$00A_H$	INTF	R/W	0000	Interrupt request flag register
$00C_H$	TCPAC	W	----	TCPA Timer/counter A control register
$00D_H$	TCPAL	W	0000	TCPA Timer/counter A data low register
$00E_H$	TCPAH	W	0000	TCPA Timer/counter A data high register
$00F_H$	PA	R	----	I/O port A data register
010_H	PB	R	----	I/O port B data register
011_H	PC	R/W	0000	I/O port C data register
012_H	PD	R/W	0000	I/O port D data register
013_H	TCPBC	W	----	TCPB Timer/counter B control register
014_H	TCPBLL	W	0000	TCPB Timer/counter B low data low nibble register
015_H	TCPBLH	W	0000	TCPB Timer/counter B low data high nibble register
016_H	TCPBHL	W	0000	TCPB Timer/counter B high data low nibble register
017_H	TCPBHH	W	0000	TCPB Timer/counter B high data high nibble register
018_H	PSP	R/W	---0	Peripheral power saving control register
019_H	PE	R/W	--00	I/O port E data register

Note: a. Default means initial value after power on or reset.
b. R is “read” only, W is “write” only, R/W is both of “read” & “write”.

§ System function description:

1. System Oscillators

The high speed oscillator can only be operated in resonator mode.

✧ Resonator/crystal mode (400K Hz~2M Hz oscillator)

A 400K Hz~2M Hz crystal across OSCI and OSCO pads, capacitors are connected between OSCI/OSCO pads and ground (VSS).

2. CPU clock

The CPU clock comes from system oscillator. In the normal operation, the system clock comes from high speed system oscillator (OSCH).

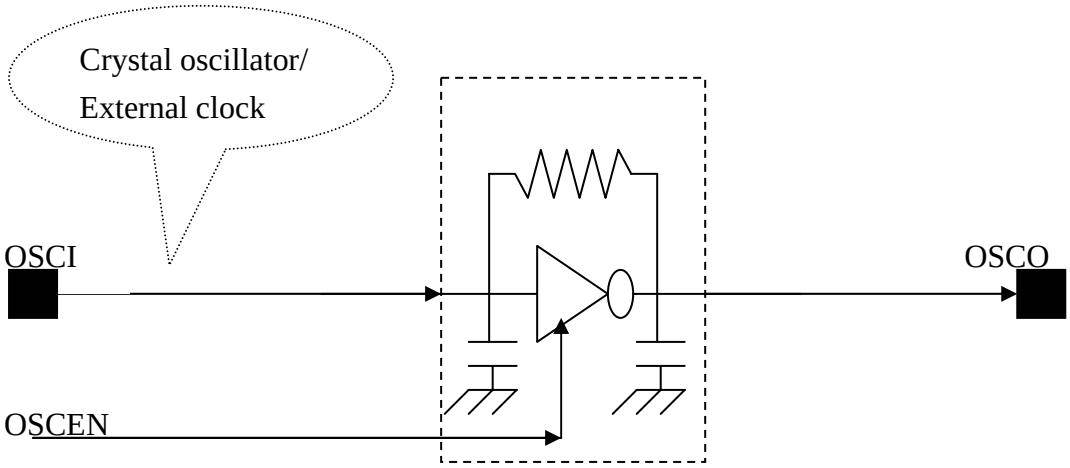


Figure: System High Speed Oscillator

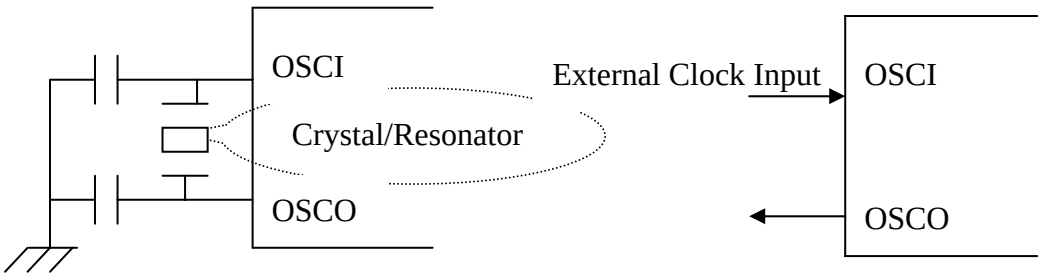


Figure: High Speed System Oscillator (OSCH)

4. Power saving mode (Stop mode)

The CPU enters stop mode is operated by writing CPU power saving register (PS). During the power saving mode, CPU holds the internal status of the system. In stop mode, the oscillator clocks will be stopped and system need a warm-up time for the stability of system clock running after wake up. As system wake up from stop mode will cause a CPU reset. Software program will restart from reset vector.

5. MCU System Operation Modes

The MCU has 2 operating modes, including high speed operation, stop modes. After power on reset, the MCU will go into high speed operation mode automatically. After wake up from stop mode, the MCU will resume the last operation mode.

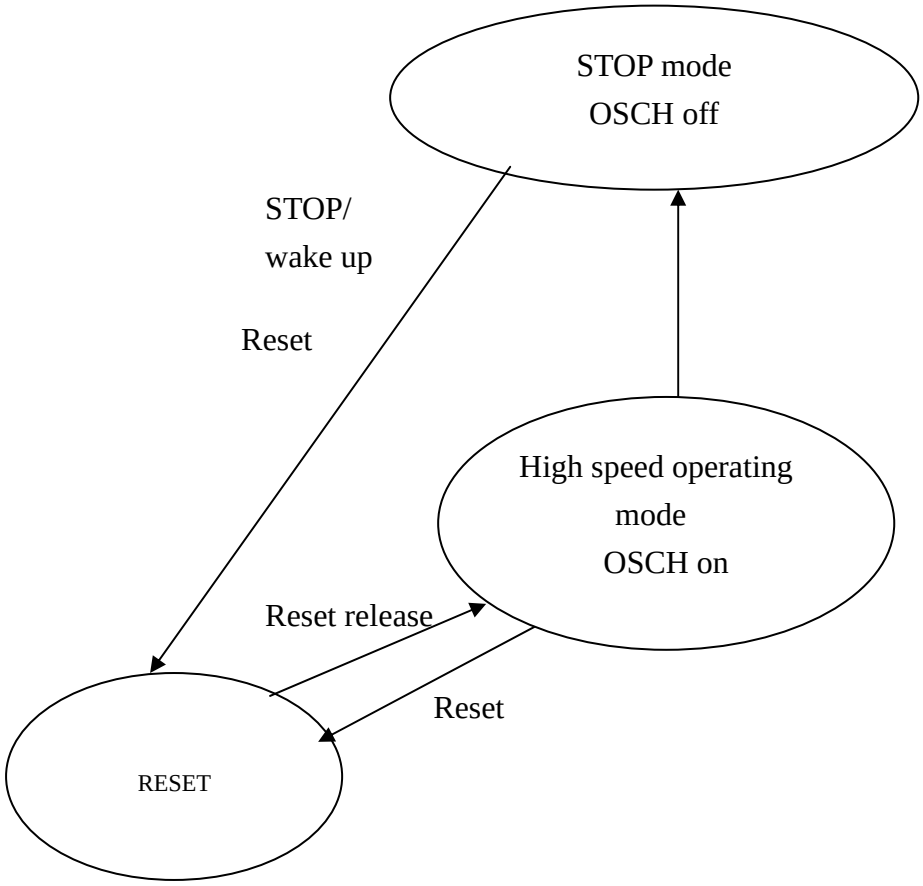


Figure: System Operation State Diagram

✧ Power saving mode condition & Release

Modes	Stop mode
Oscillator	**Stopped**
CPU internal status	Program counter, stack, flag register reset
Program counter	Reset as $0000
Peripherals: Timers, Interrupts, Register, I/O PC & PD	Stopped & Retain Output data cleared
Watch Dog Timer	Disable & cleared
Release Condition	Reset, Input wake-up

✧ PS: Power saving register[R/W] , default value [---0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	STOP
Read/write	-	-	-	R/W

STOP: Into stop mode. (0: inactive; 1: active)

✧ PSP: Peripheral power saving register[R/W] , default value [---0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	IROEN
Read/write	-	-	-	R/W

IROEN: IRO output enable (0: disable; 1: enable)

The system oscillator generates the system control timing for CPU core or peripheral devices with fixed control phase, so the waveform of oscillator becomes sensitive to noise, abnormal duty especially fatal for CPU. Any switching of clock source needs oscillation stable time (OST) to make sure the oscillation is stable and synchronized with CPU timing phase. The OST is 512's RC16K clocks with reference value as below table:

6 .Interrupts

The CPU provides only 1 interrupt vector ($001H) and no priority, but can expand to multi-sources. Interrupt source includes two timer/counter interrupts (TCPAINT &TCPBINT). The interrupt control registers (INTC) contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTF) registers. Before finishing the INT service routine, another INT request will keep waiting until program return from interrupt routine.

✧ INTC: Interrupt control register [R/W], default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TCPBIE	TCPAIE
Read/Write	-	-	R/W	R/W

TCPAIE: Enable interrupt of timer/counter A. (0: disable; 1: enable)

TCPBIE: Enable interrupt of timer/counter B. (0: disable; 1: enable)

✧ INTF: Interrupt request flag register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TCPBF	TCPAF
Read/Write	-	-	R/W	R/W

TCPAF: Timer/counter A' interrupt request flag. (0: inactive; 1: active)

TCPBF: Timer/counter B' interrupt request flag. (0: inactive; 1: active)

If the interrupt request needs service, the programmer may set the corresponding INT enable bit to allow interrupt active. The internal timer/counter interrupt is setting the TCPxF to 1, resulting from the timer/counter overflow.

When the corresponding interrupt enable and flag bits is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then proceeds with the relative interrupt service. After CPU writes the corresponding bits to 0 in the INTF register, the service flag will be cleared to 0(using STX #n, $m instruction). The INTF registers' bit can only write "0" to clear the flag. User writes "1" to Flag bit with no effect.

OST	From Stop state	oscillating	Unit
System clock(OSCH) Crystal/Resonator	4	4	OSCH clock

7. Watch Dog Timer (WDT)

The clock of watch dog timer comes from timer A' PFD. User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watchdog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides 2 steps clear watchdog command as the programmer writes INTF with $F data first that will enable the WDT clear, and then writes the power saving (PS) control register after. Completely finishes the two write steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop. *User should keep in minds that always reset WDT at main program and never clear the WDT in the interrupt routine.*

The max period of WDT = (TB1OV cycle time) * 8

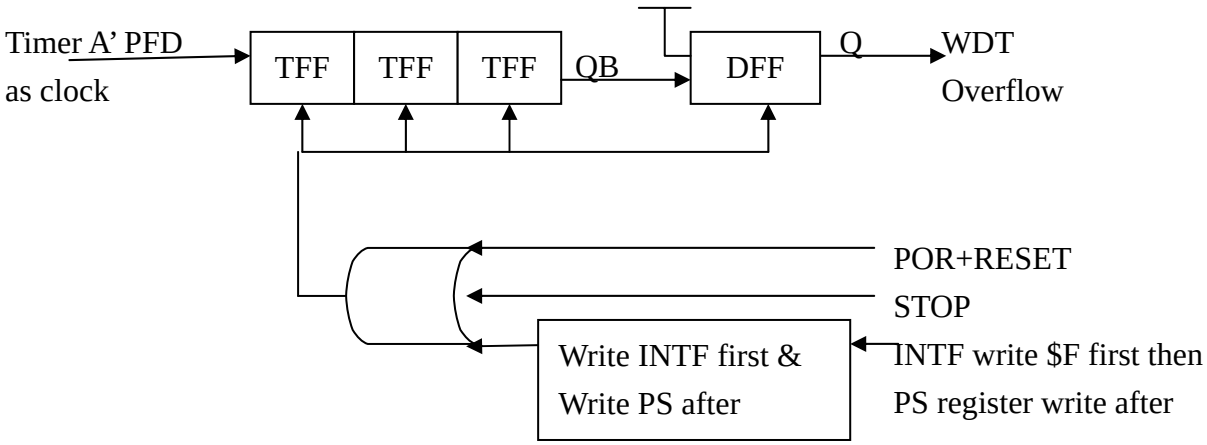


Figure: Watch Dog Timer control circuit

8. RESET

The chip has three kinds of reset sources: POR (power on reset), Watch dog timer reset, LVR (low voltage reset). The reset feature can be divided into 2 kind groups that one is system reset and the other is CPU reset. The system reset will initialize the CPU and peripheral device with default state. The CPU reset only initializes the CPU state and keeps the peripheral state no change.

S-8a System reset

.POR (power on reset)

The chip provides automatic reset function when the power is turned on. The VDD should be below 1.4V and its rising slope (from 0.1VDD up to o.9VDD) needs less than 10ms.

S-8b CPU reset

.Watch Dog Timer Reset

The reset signal will generate automatically when the watchdog timer runs overflow. If the watchdog timer is cleared regularly by user's program, no watchdog reset will occur. Unless the MCU is forced into abnormal state, the software controlled procedure is disrupted and causing watch dog timer overflow, then it will generate reset signal to initializes the chip returning to normal operation.

. **LVR (low voltage reset)**

LVR	System RESET	Detected Vop
0→1	active	1.2V~1.8V
1→0	disable	>1.8V

The LVR is a low system voltage detector. As the operating voltage falls below the detected window then the system reset will start the system reset procedure.

For OTP type, hardware needs to down load the mask options into register and the events are caused by power on reset, watch dog overflow reset and LVR reset.

§ Peripheral function description:

1. 8 bits Carrier Timer (TCP) for TCPB

One 8-bits timer (TCP) with system clock source and preload data buffer can implement as a timer, IRO is programmable frequency divider can support IR carrier generator. TCPOV is the timer overflow signal and the rising edge will set the relative INT flag.

✧ TCPC: Timer control register[W], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	-
Read/Write	-	-	-	-

As writing the TCPC address, the timer will reload the high latch data into counter that means PFD will be initialized for choosing high latch data.

✧ TCPDLL: TCP low nibble for low data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPDL3	TCPDL2	TCPDL1	TCPDL0
Read/Write	W	W	W	W

TCPD3~TCPD0: TCPD low nibble of data buffer.

✧ TCPDLH: TCP high nibble for low data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPDL7	TCPDL6	TCPDL5	TCPDL4
Read/Write	W	W	W	W

TCPD7~TCPD4: TCPD high nibble of data buffer.

✧ TCPDHL: TCP low nibble for high data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPDH3	TCPDH2	TCPDH1	TCPDH0
Read/Write	W	W	W	W

TCPDH3~TCPDH0: TCPDH low nibble of data buffer.

✧ TCPDHH: TCP high nibble for high data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPDH7	TCPDH6	TCPDH5	TCPDH4
Read/Write	W	W	W	W

TCPDH7~TCPDH4: TCPDH high nibble of data buffer.

✧ TCPDL: Like a 8 bit TCP low data register, default value [00H]

TCPDL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPDL7	TCPDL6	TCPDL5	TCPDL4	TCPDL3	TCPDL2	TCPDL1	TCPDL0

✧ TCPDH: Like a 8 bit TCP high data register, default value [00H]

TCPDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPDH7	TCPDH6	TCPDH5	TCPDH4	TCPDH3	TCPDH2	TCPDH1	TCPDH0

.Timer

When TCP works as a Timer, user needs give the preload data TCPDH (output high level)/TCPDL (output low level) for periodic waveform generation. After initial setting, user starts the TCP counting by setting TCPEN=1, the TCP cycle period is:

Tc = (selected clock cycle) * (TCPDH+TCPDL)

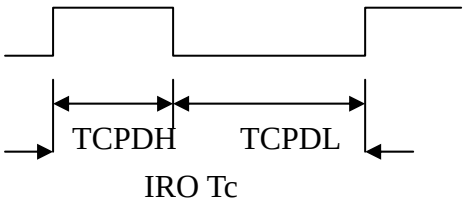
When user writes data to the TCPDH & TCPDL, the data just keep in TCPDxL/H register. During the TCPEN=1 command executed, the TCPD 1's complement value will load the TCPDHx into counter TCP as initial value and start the timer function. Necessary keeps in auto reload mode, timer run with reload feature as TCP up counts and reaches the value 0f "FF_H" or 255. The next reload data is TCPDLx for carrier low level. The procedure keeps alternately and Infrared carrier generation & PWM output are easily implemented.

.IRO

The IRO Mode includes in timer mode and the output frequency is:

IRO frequency= (selected clock frequency) / (TCPDH+TCPDL)

At this time, most users will disable the interrupt feature for tone or melody generation.



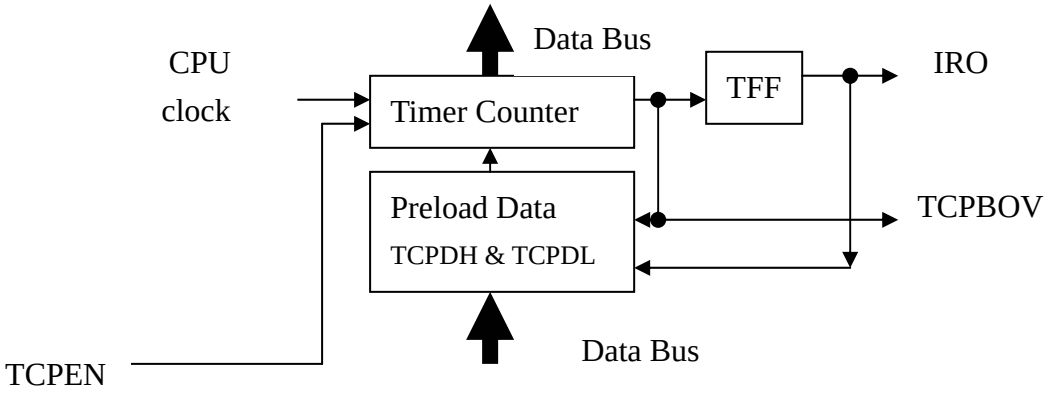


Figure: 8 bits Timer for IRO

2. 8 bits Timer/Counter (TCP) for TCPA

One 8-bits timer (TCP) with IRO clock source and preload data buffer can implement as a timer feature. TCPOV is the timer r overflow signal and the rising edge will set the relative INT flag.

✧ TCPC: Timer/counter/PFD control register[W], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	-
Read/Write	-	-	-	-

As writing the TCPC address, the timer will reload the latch data into counter.

✧ TCPDL: TCP low nibble data register[W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPD3	TCPD2	TCPD1	TCPD0
Read/Write	W	W	W	W

TCPD3~TCPD0:TCPD low nibble of data buffer.

✧ TCPDH: TCP high nibble data register[W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPD7	TCPD6	TCPD5	TCPD4
Read/Write	W	W	W	W

TCPD7~TCPD4: TCPD high nibble of data buffer.

✧ TCPD: Like a 8 bit TCP data register[W], default value [00H]

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPD7	TCPD6	TCPD5	TCPD4	TCPD3	TCPD2	TCPD1	TCPD0
Read/Write								

.Timer

When TCP works as a Timer, user needs give the preload data TCPD for periodic interrupt. After initial setting, user starts the TCP counting by setting TCPEN=1, the TCP cycle period is:

Tc = (selected clock cycle) * (TCPD)

When user writes data to the TCPD, the data just keep in TCPDL/H register. During the TCPEN=1 command executed, the TCPD 1's complement value will load into counter TCP as initial value and start the timer function. Necessary keep in the auto reload mode, timer run with reload feature as TCP up counts and reaches the value 0f "FF_H" or 255. At the same time, interrupt request flag TCPF will set activated, if software enables the corresponding interrupt enable bit, INT hardware will cause MCU interrupt service routine.

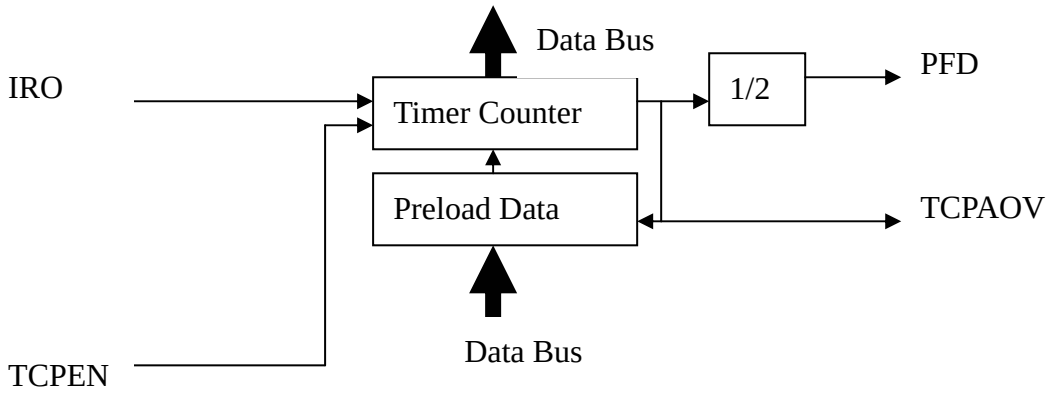


Figure: Timer/Counter

.. IO Pad Cells

The main features of pad cell are including ESD/EFT protection and general I/O access. An open drain I/O pad cell can be used as input with or without pull-up resistor, or working as a CMOS or NMOS output driver. The input pad cell must have pull-up resistor for avoiding a floating state when user doesn't care or not be used. For concerning the standby current, user can use data register or I/O control register to fit the application.

. I/O File Register

✧ PA: Port A input port [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PA3	PA2	PA1	PA0
Read/Write	R	R	R	R

PA3~PA0: port A' input port.

✧ PB: Port B input port [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PB3	PB2	PB1	PB0
Read/Write	R	R	R	R

PB3~PB0: port B input port.

✧ PC: Port C data register [R/W], default value [0000]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PC3	PC2	PC1	PC0
Read/Write	R/W	R/W	R/W	R/W

PC3~PC0: port C data register NMOS output only.

✧ PD: Port D data register [R/W], default value [0000]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PD3	PD2	PD1	PD0
Read/Write	R/W	R/W	R/W	R/W

PD1~PD0: port D data register. NMOS output only

PD3~PD2: port D data register. With CMOS or NMOS output optional.

✧ PE: Port E data register [R/W], default value [--00]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	-	-	PE1	PE0
Read/Write	-	-	R/W	R/W

PE1~PE0: port E data register NMOS output only.

. I/O PAD Cell Structure & Function Description

.. Input Port

The input port always has the pull high resistor and input data can read by port reading command. A wake-up function also offers the system wake up feature for keys or special external triggers.

Input Data	**Read Data**	**Wake-up**
0	**0**	**Active**
1	**1**	**Non-active**
Floating	**1**	**Non-active**

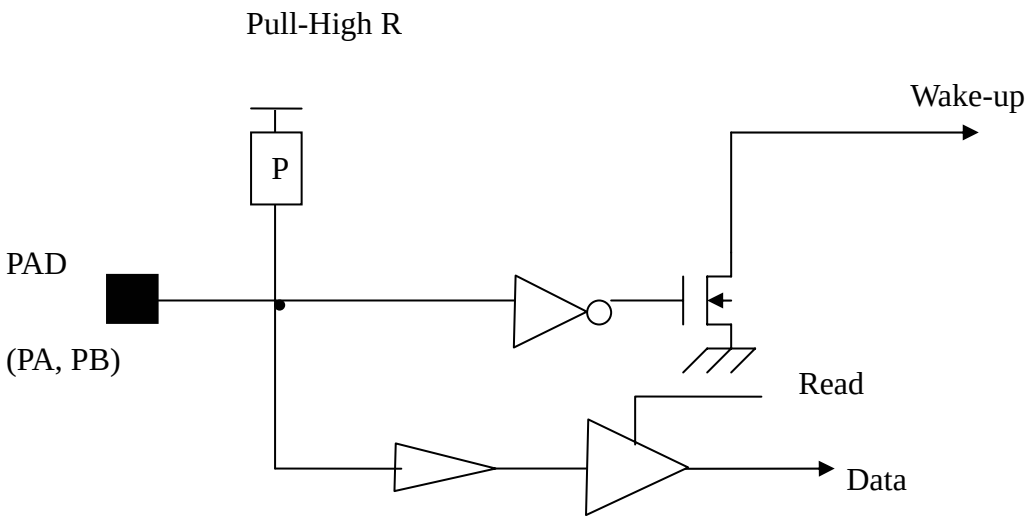


Figure IO-E: Input Port

.. Output Port

The output driver has drive capability for heavy load. The output enable option is a control signal for disable output feature and pad can release to use as input or another request.

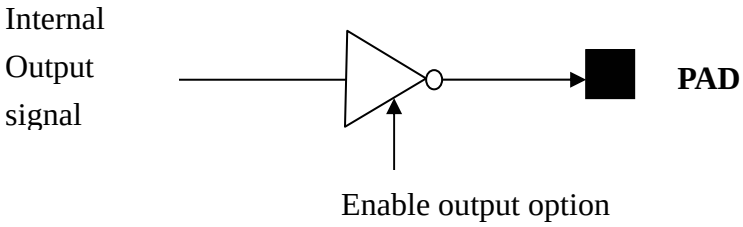


Figure IO-G: Output Driver Port

Internal signal Data	Output option enable	**PAD Data**
x	disable	**Floating**
0	enable	**0**
1	enable	**1**

.. Standard open drain IO Port

The standard open drain IO port has no I/O control register for switching input or output mode and use output data register to change the IO mode. If output data=1, the I/O port is programmed as input with pull-up resister or not dependant on CMOS type or NMOS type output.

Output Type	Output Register data	PAD data	**Pull-up**
CMOS	0	0	**No**
CMOS	1	Input mode	**Yes**
NMOS	0	0	**No**
NMOS	1	Input mode	**No**

Note: In the STOP mode IO port data register will be cleared that is for key scan with wake up feature.

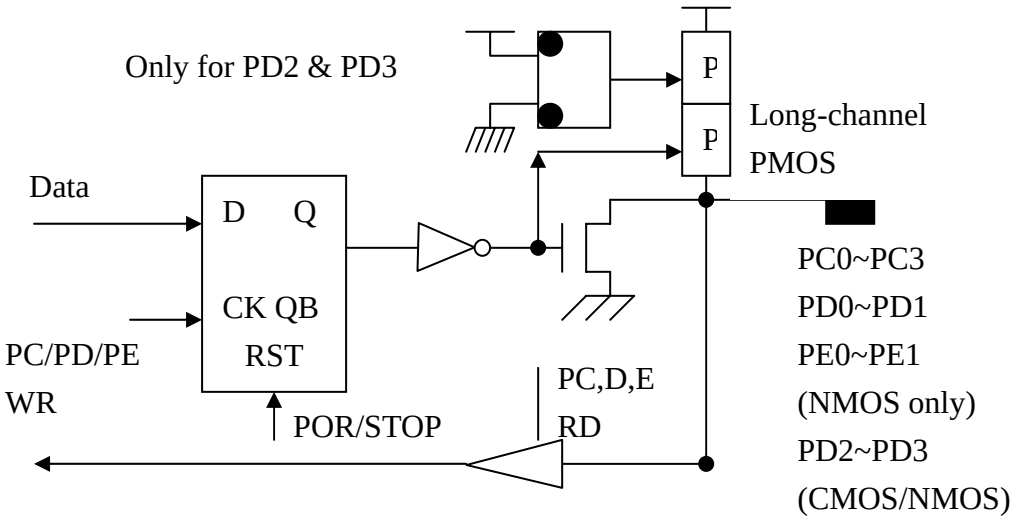


Figure IO-F: Standard open drain IO Port

§ Mask Option Table:

✧ MOPTION: Mask option register [R/W], default value [-00-]

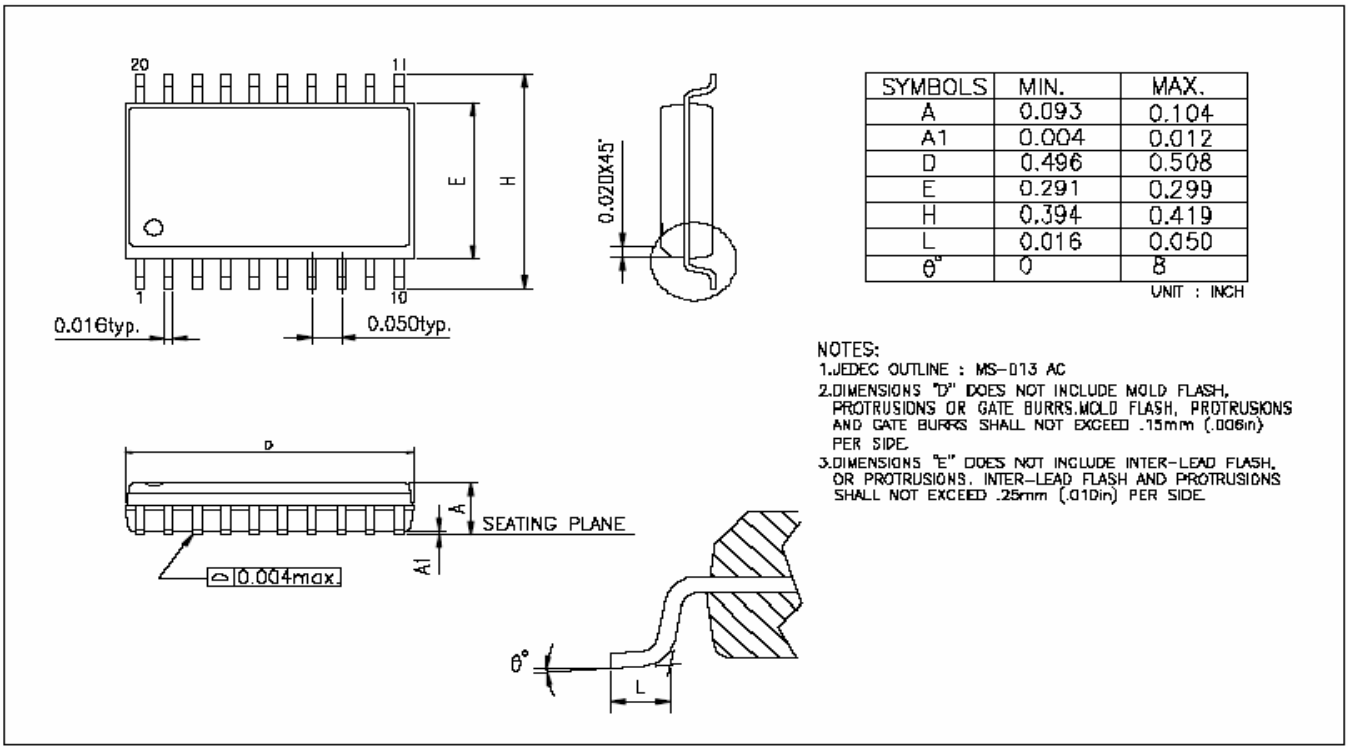
Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	-	PD3	PD2	-
Read/Write	-	R/W	R/W	-

PD2: "0" is NMOS output or "1" is CMOS type output for PD2

PD3: "0" is NMOS output or "1" is CMOS type output for PD3

§ Package & PAD Information:

20-SOP

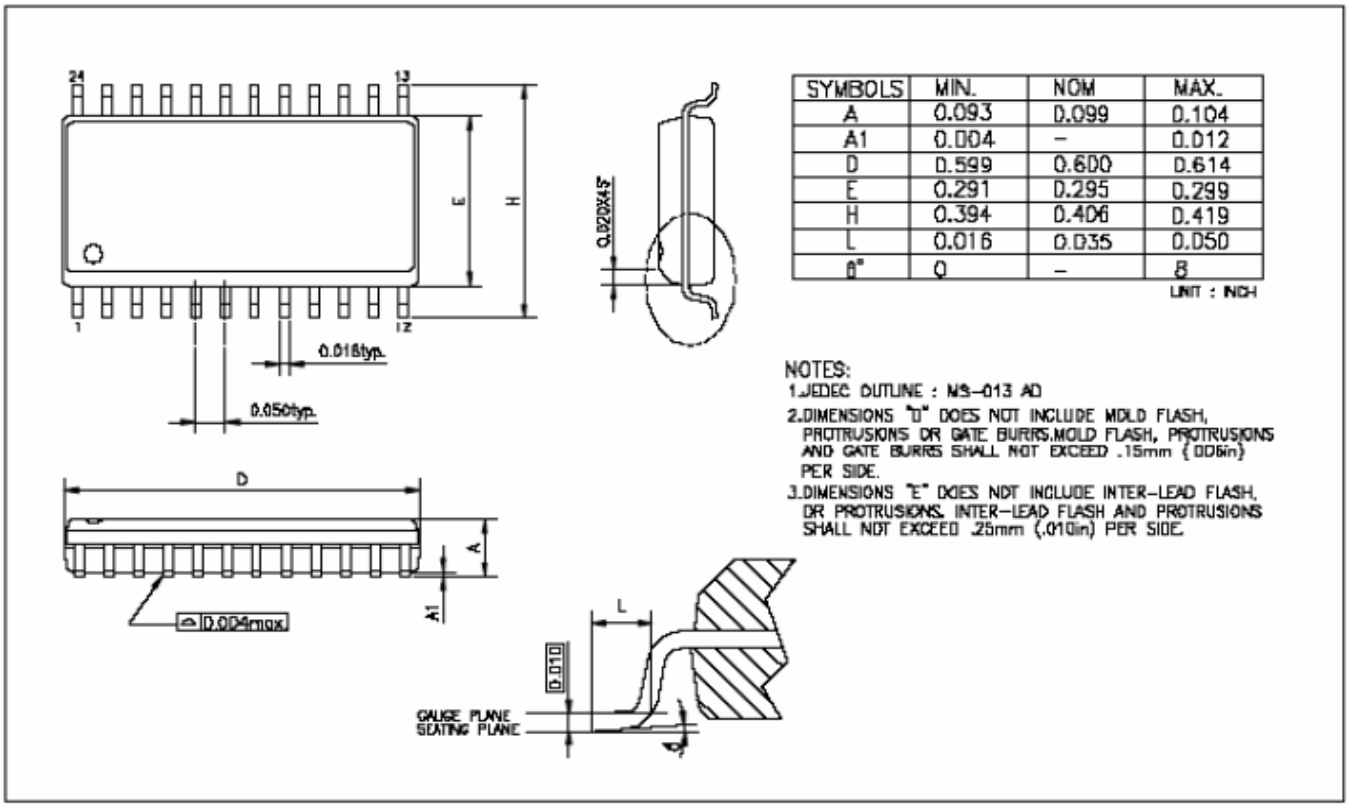


SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.496	0.508
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-013 AC
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

24-SOP

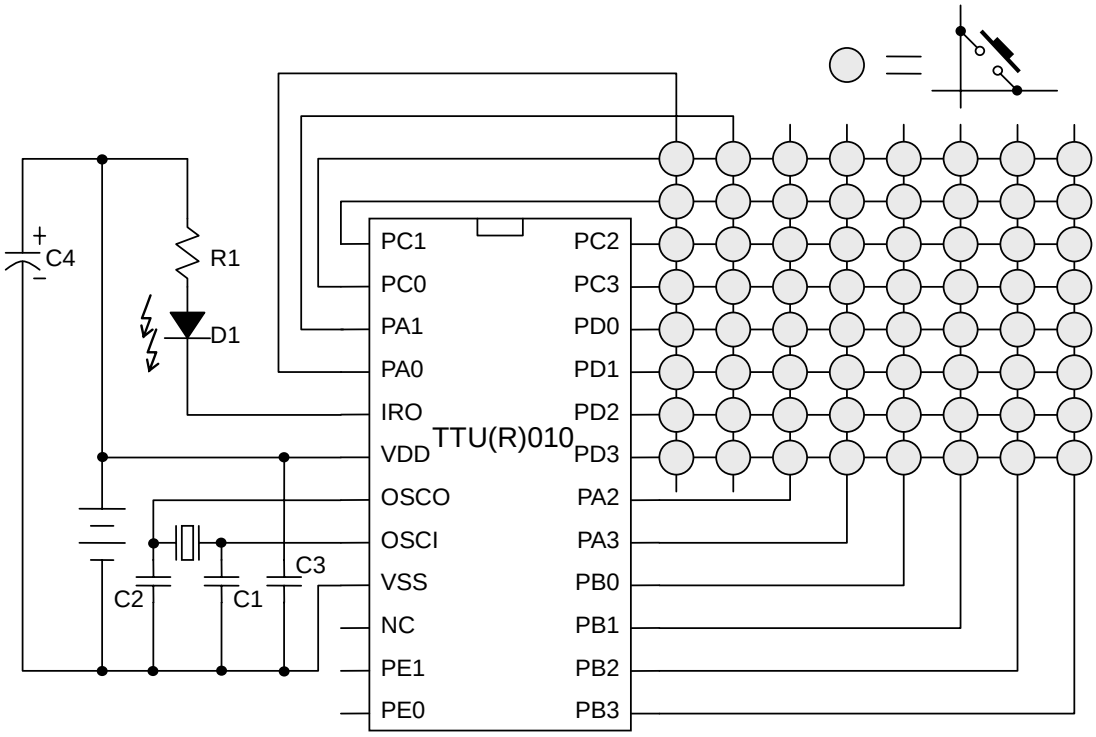


SYMBOLS	MIN.	NOM	MAX.
A	0.093	0.099	0.104
A1	0.004	–	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	–	8

UNIT : INCH

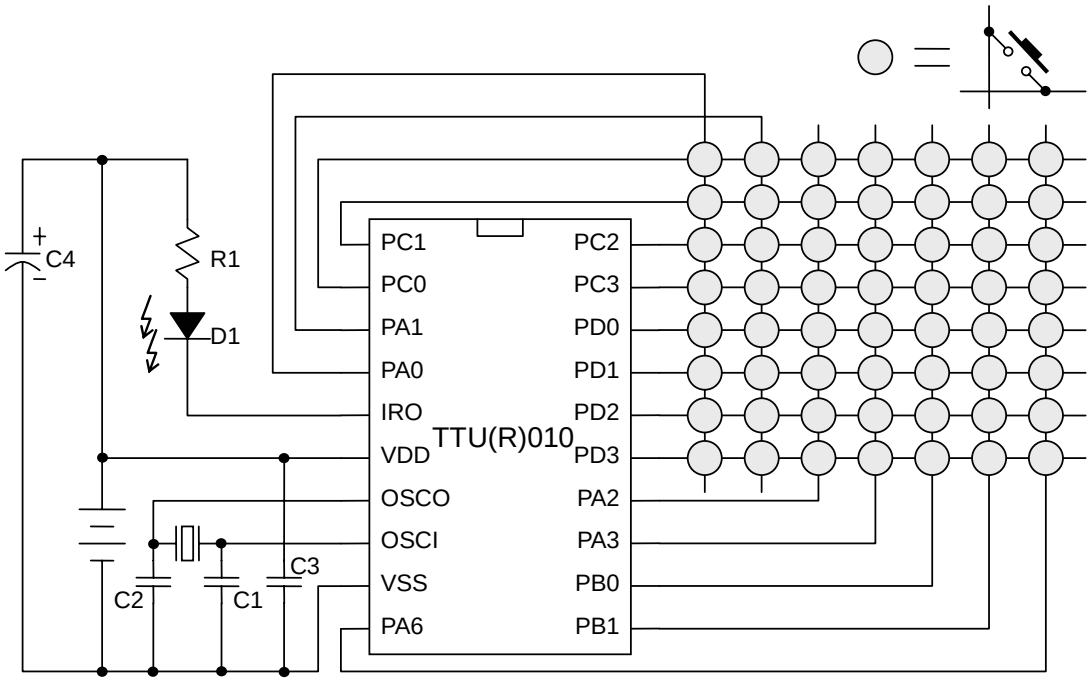
NOTES:
1.JEDEC OUTLINE : MS-013 AD
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

§ Application Circuit



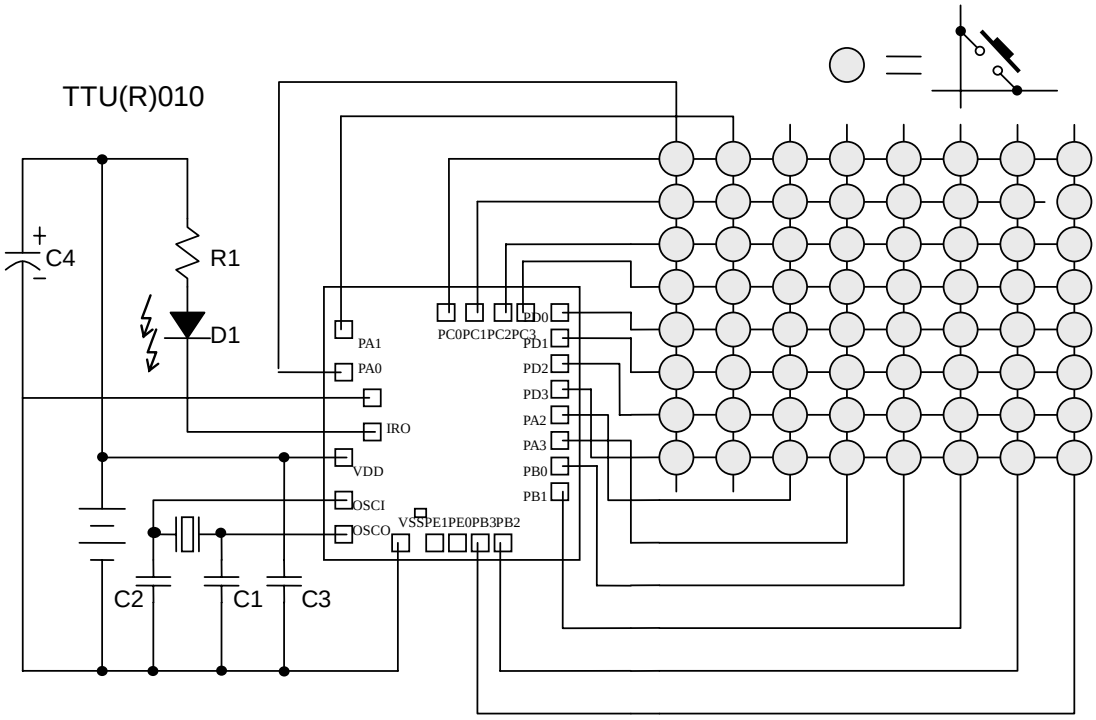
24 SOP application circuit example

Device	Recommended constant
R1	3.3~10 Ω
C1, C2	100~300 pF for 455kHz ceramic resonator application
	3~30 pF for 4MHz resonator or crystal application
	Unnecessary for C-containing resonator application
C3	0.1 μF
C4	4.7 μF
D1	IR LED



20 SOP application circuit example

Device	Recommended constant
R1	3.3~10 Ω
C1, C2	100~300 pF for 455kHz ceramic resonator application
	3~30 pF for 4MHz resonator or crystal application
	Unnecessary for C-containing resonator application
C3	0.1 μF
C4	4.7 μF
D1	IR LED



DICE application circuit example

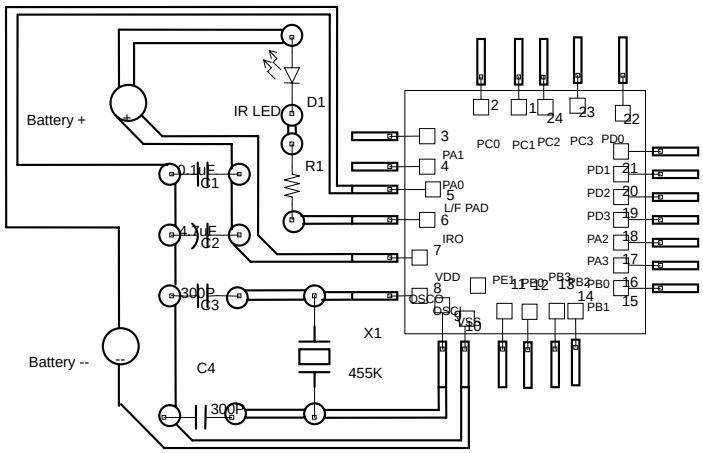
Device	Recommended constant
R1	3.3~10 Ω
C1, C2	100~300 pF for 455kHz ceramic resonator application
	3~30 pF for 4MHz resonator or crystal application
	Unnecessary for C-containing resonator application
C3	0.1 μF
C4	4.7 μF
D1	IR LED

§Appendix:

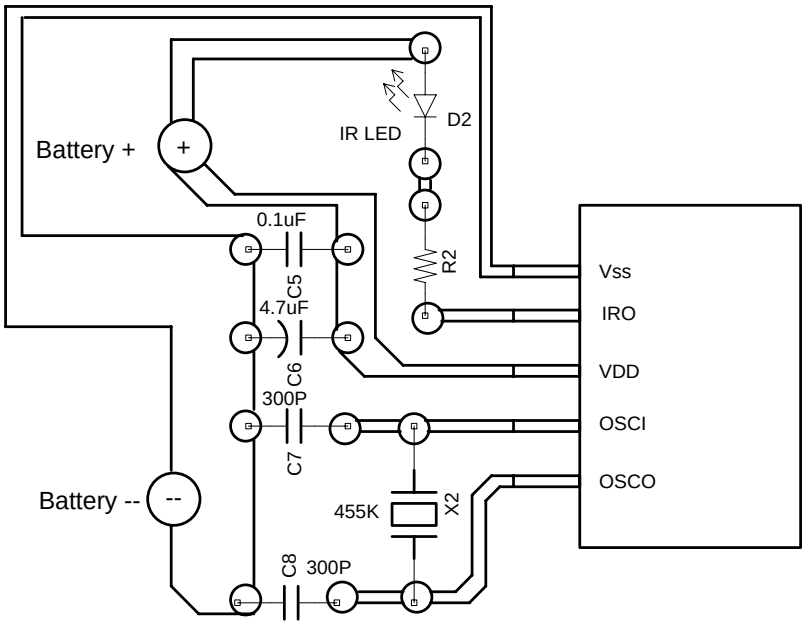
For the remote control application, the IR transmission may cause the variations in current from a few hundred uA to a few hundred mA. This current variation will generate overshoot and undershoot noise on the power line to cause the system malfunction.

To reduce the noise and stabilize the operation of the chip, we recommend the application designer design the PCB for the remote controller as follows to reduce the overshoot and undershoot of the IR LED drive current.

- ✧ Oscillator circuit (resonator & capacitors) should be located as near as possible to the chip
- ✧ PCB pattern for V_{DD} & V_{SS} should be as wide and short as possible
- ✧ IR LED should be located as far as possible from the chip
- ✧ Power supply battery and power capacitor (0.1uF & 47uF) should be located as near as possible to the chip
- ✧ The V_{DD} pattern of the IR LED and the power pins of the chip (V_{DD} & V_{SS}) should be separated and connected directly with the battery terminal
- ✧ The power capacitors (0.1uF & 47uF) is recommend to reduce the noise
- ✧ Keeping substrate floating and L/F pad connects to V_{SS} power line in dice form
- ✧ The recommended R1/R2 is 15Ω



Recommended PCB layout for dice



Recommended PCB layout for package

§ Ordering Form:

a. Package form : TTU(R)010-zzz
b. Chip form : TCU(R)010-zzz
c. Wafer base : TDU(R)010-zzz

§ Modified Record:

Date	Name	Version	Page	Content
2007/3/22	Hans Yang	v0.0-000	1~32	Preliminary
2007/3/29	Hans Yang	V0.0-000	6	Correct IRO Sink Current.
2007/4/3	Hans Yang	V0.0-000	6	PD2,PD3 replace PC,PD,PE
			1,20,23	Distinguish only PD2 & PD3 with CMOS and NMOS option
2007/4/27	Hans Yang	V0.0-001	3,13	Block Diagram, WDT
2007/5/7	Hans Yang	V0.0-001	9,16,19	Timer A & B write only
2007/5/10	Hans Yang	V0.0-001	11,12,13	Omit Sleep, INT1C & INTF
2007/5/15	Hans Yang	V0.0-001	1,7	RAM: 48X4
2007/5/22	Hans Yang	V0.1-000	6,26,27,28	cancel 4M & 3.64M spec
2007/5/31	Hans Yang	V0.1-000	1,6,7	Separate operating voltage for different frequency
2008/2/19	Hans Yang	V2.0-000	1,6,7	Cancel Separate operating voltage for different frequency