TTU261L Target Spec

General Description:

TTU261L is a 4-bit T416 microcontroller. It contains 1K*16 ROM, 48*4 RAM and up to 48-dots LCD drivers, which is designed for LCD products application. The device is suitable for application in family appliance, consumer product, particularly in watch, timer, counter & pedometer application.

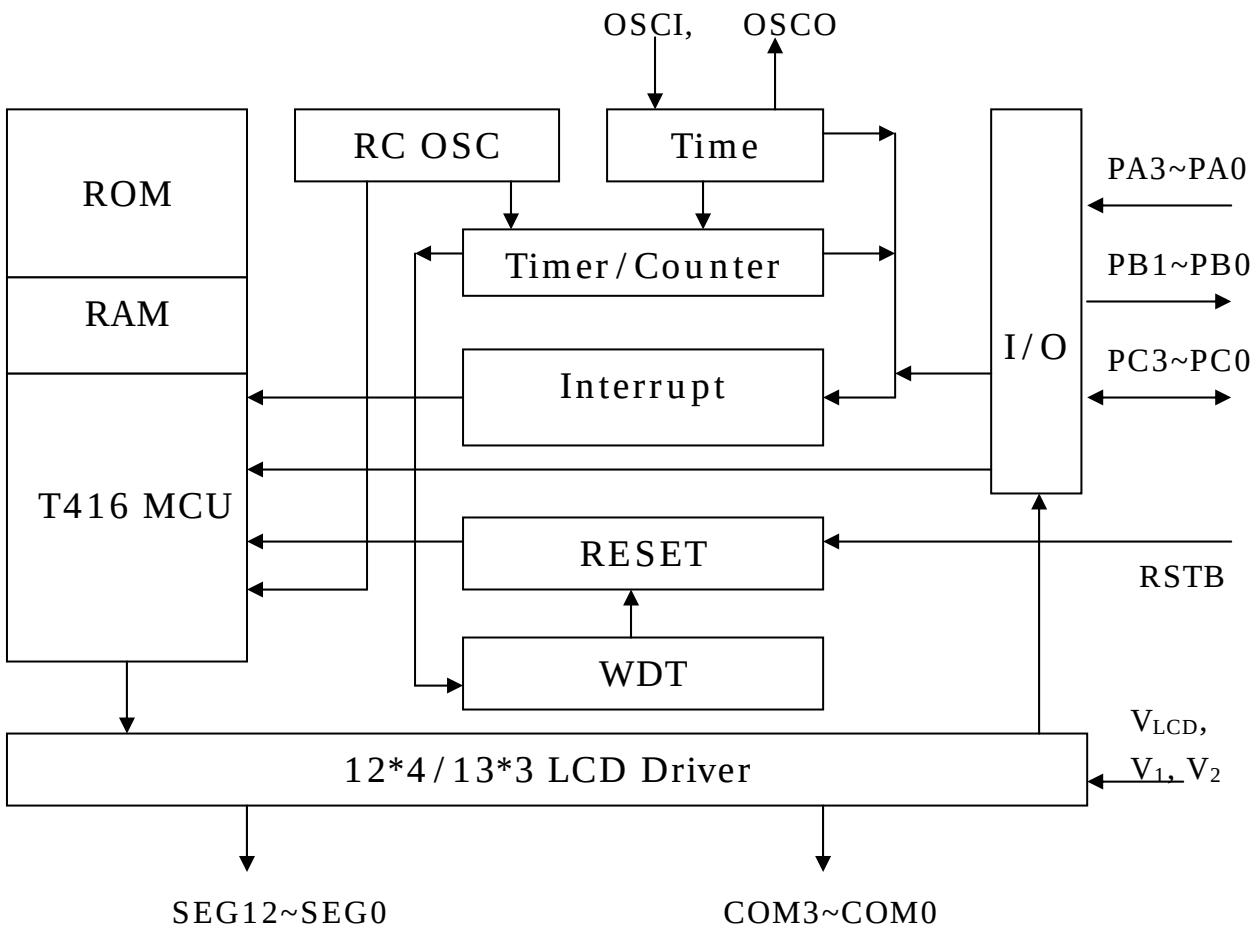
Features:

1. 4-bit T416 MCU core
2. 2-level stack
3. Operating voltage: 1.2V~1.8V
4. Operating frequency:
   - ✧ 128KHz/32KHz @1.5V
5. Built-in 32768Hz crystal oscillator & internal RC oscillator
6. 1K*16 program ROM
7. 48*4 SRAM
8. 4 I/P pins, 2 O/P pins & 4 general programmable I/O pins
   - ✧ Input port key wake up by mask option
   - ✧ Buzzer frequency selected by mask option
   - ✧ PA0 can be used as timer/counter input
   - ✧ PA1 latch type trigger
9. 48/39 dots LCD display optioned by mask
   - ✧ 12*4 LCD driver (1/4 duty; 1/2 bias)
   - ✧ 13*3 LCD driver (1/3 duty; 1/2 bias)
10. One 8-bit auto-reload timer/counter
11. Built-in software control for power saving function
12. Built-in watch dog timer reset circuit
13. Provides 4 interrupt sources
    - ✧ External: PA0, PA1
    - ✧ Internal: Timer/counter, Base timer

Applications:

- ✧ LCD products
- ✧ Watch/ Timer
- ✧ Counter/ Step counter/ Pedometer

Block Diagram:



Pin Description:

Pin Name	I/O	Description
V_{DD}		Positive power supply
V_{SS}		Negative power supply, ground
OSCI	I	32768Hz crystal input, can be connected to crystal
OSCO	O	32768Hz crystal output, can be connected to crystal
PA3~PA0	I	4-bits input port, PA0 can be used as 8-bit timer/counter clock source & external interrupt. PA1 can be defined as external interrupt (latch type). PA3 & PA2 used as general input pins. All PA pins can be defined as keyboard wakeup & pull-high resistor by mask.
PB1/SEG12 PB0/SEG11	O	LCD segment driver outputs or general output ports, determined by mask option
PC3~PC0	I/O	Bidirectional 4-bits I/O port, PC1 & PC0 can be used as buzzer output or general I/O port. PC3 & PC2 used as general I/O pins.
SEG10~SEG1	O	Segment drivers for LCD display
COM3/SEG0	O	Common driver (COM3) or segment driver (SEG0) for LCD display selected by mask option.
COM2~COM0	O	Common drivers for LCD display
V_{LCD}, V_1, V_2		C type double pump
RSTB	I	External reset input, active low, internal pull-high resistor

DC Characteristics: (V_{DD}=1.5V, Ta=25°C)

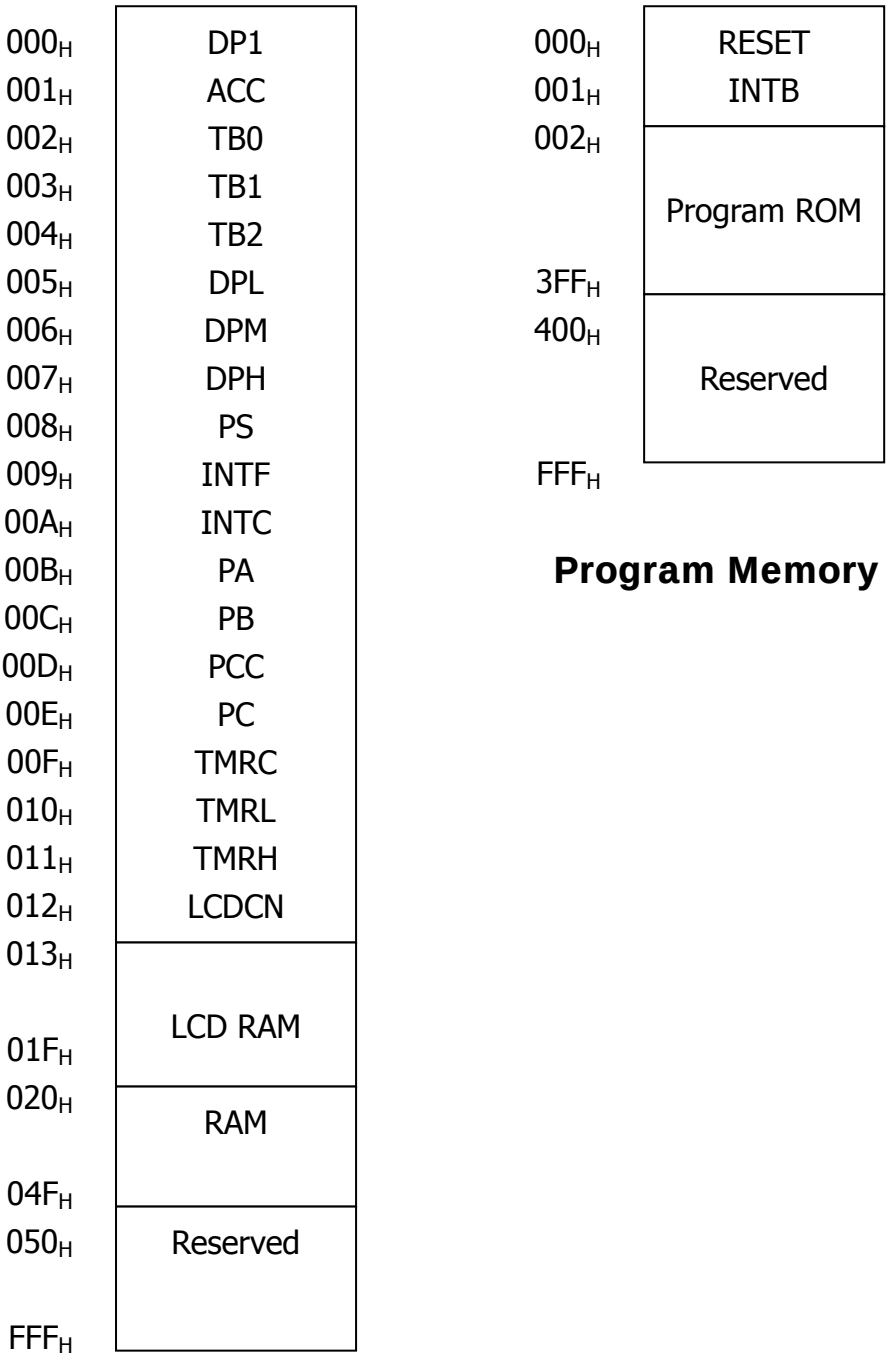
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	F_{CPU}=128KHz	1.0	1.5	1.8	V
Operating Current	I_{DD1}	F_{CPU}=128KHz, F_{SYS}=32768Hz, I/O no load, LCD on	-	32	-	uA
	I_{DD2}	F_{CPU}=32KHz, F_{SYS}=32768Hz, I/O no load, LCD on	-	14	-	
	I_{DD3}	F_{CPU}=STOP, F_{SYS}=32768Hz I/O no load, LCD on	-	5	-	
Standby Current	I_{STB}	I/O no load, All OSC stop	-	-	1.0	uA
PA3~PA0, PC3~PC0 Input Low Voltage	V_{IL}		0	-	0.2	V_{DD}
PA3~PA0, PC3~PC0 Input High Voltage	V_{IH}		0.8	-	1.0	V_{DD}
PB1, PB0, PC3~PC0 Sink Current	I_{OL}	V_{DD}=1.5V, V_{OL}=0.5V	1.0	2.0	-	mA
PB1, PB0, PC3~PC0 Source Current	I_{OH}	V_{DD}=1.5V, V_{OH}=1.0V	-1.0	-2.0	-	mA
SEG Output High Voltage	V_{OH1}		2.8	-	-	V
SEG Output Low Voltage	V_{OL1}		-	-	0.2	V
COM Output High Voltage	V_{OH2}	I_{OH}=-1mA	Vdd-1	-	-	V
COM Output Low Voltage	V_{OL2}	I_{OL}=1mA	-	-	0.8	V
PA3~PA0, PC3~PC0, RSTB Pull-High R	R_{PH}	V_{DD}=1.5V	100	150	200	KΩ
Oscillator Start up voltage	V_{ST}	F_{SYS}=32KHz	1.0	-	-	V
Oscillator Sustain voltage	V_{SU}	F_{SYS}=32KHz	0.8	-	-	V

AC Characteristics:

Parameter	Test Condition		Min	Typ	Max	Unit
Oscillator Frequency	F_{CPU}	V_{DD}=1.5V	-	128/32	-	KHz
System Frequency	F_{SYS}	V_{DD}=1.5V	-	32.768	-	KHz
System Startup Period	T_{CPU1} (128KHz/32KHz)	Power-up or wake-up from STOP mode	-	512	-	F_{CPU}
	T_{CPU2} (128KHz/32KHz)	wake-up from SLEEP mode	-	64	-	
System Stable Period	RC from 128KHz to 32KHz		-	8	-	F_{CPU}
	RC from 32KHz to 128KHz		-	64	-	

Functional Description:

Map of Memory and I/O



Data Memory **Program Memory**

Memory Map

000_H~$3FF_H$	Program ROM [1K*16]
013_H~$01F_H$	LCD RAM [48/39 dots]
020_H~$04F_H$	Internal RAM [48*4]

✧ CPU Control Register

Address	Symbol	R/W	Default	Description
000_H	DP1			
001_H	ACC			
002_H	TB0			
003_H	TB1			
004_H	TB2			
005_H	DPL			
006_H	DPM			
007_H	DPH			
008_H	PS	R/W	0000	CPU power saving register
009_H	INTF	R	0000	Interrupt request flag register
$00A_H$	INTC	R/W	0000	Interrupt control register
$00B_H$	PA	R	----	Input port A register
$00C_H$	PB	R/W	0000	Output port B register
$00D_H$	PCC	R/W	1111	I/O port C control register
$00E_H$	PC	R/W	1111	I/O port C register
$00F_H$	TMRC	R/W	0000	Timer control register
010_H	TMRL	R/W	0000	Timer data low register
011_H	TMRH	R/W	0000	Timer data high register
012_H	LCDCN	R/W	0000	LCD control register

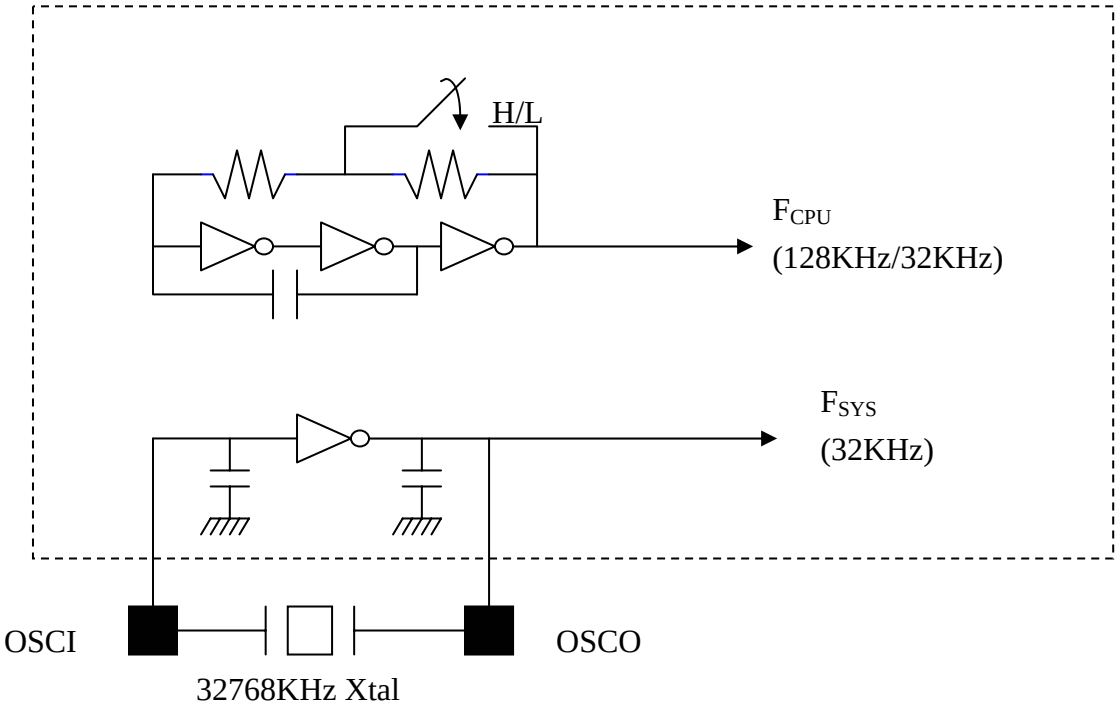
1. Oscillators

✧ 32768 oscillator for system clock

A 32768Hz crystal across OSCI and OSCO, no capacitors are connected between OSCI/OSCO and ground. The 32768Hz frequency has provided as peripheral system clock (F_{SYS}).

✧ Internal RC oscillator (128K/32KHz)

The chip was built in an internal 128K/32K Hz RC oscillator which is selected by H/L bit in PS register for T416 as CPU clock.



2. Timer/Counter

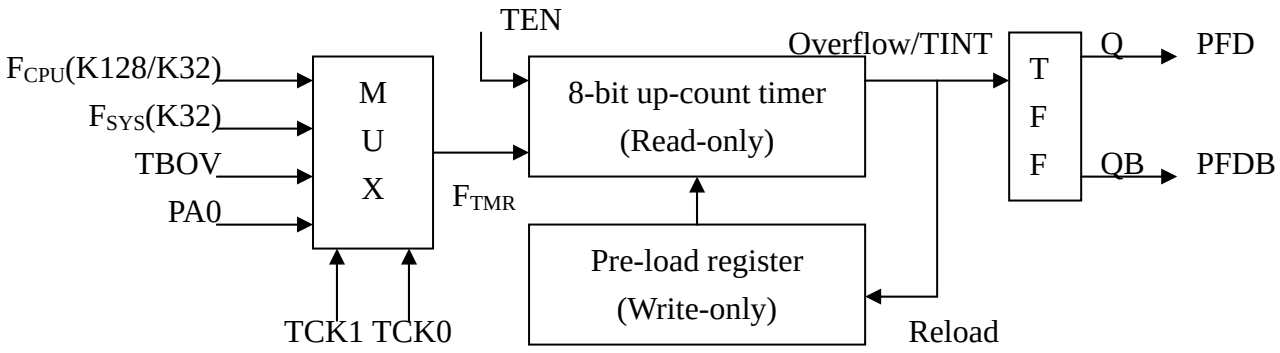
The chip has one 8-bit timer. The timer consists of an 8-bit counter and an 8-bit preload register. The timer/counter clock source comes from F_{CPU}(K128/K32), F_{SYS}(K32), TBOV (base timer overflow) or PA0 (external port A), determined by TMRC register.

Write TMRH(L) register only the data into pre-load register. The data in the pre-load register will be changed when writing TMRH[L]. The timer starts into counting when writing TMRC register bit0 “TEN” to 1 enables the timer, otherwise the timer is on the off-duty situation.

Timer counts the current contents and generates an overflow flag. For example, the programmer writing “FE_H” into timer/counter will count 254 times timer clock and generate an overflow flag at the same time. The content “00_H” will count 256 clocks. When the overflow interrupt generates will also reload the contents in the pre-load register into timer.

Writing data to pre-load high nibble register will also reload the data into timer in the timer “OFF-COUNT” condition. When the timer is counting, writing data will only keep into the pre-load register. The timer will still operate until overflow and then reload the new data into timer.

The H/L bit will determine the F_{CPU} frequency is 128KHz or 32KHz.



✧ TMRC[$00F_H$], Timer control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TCK1	TCK0	BZEN	TEN

TCK1 & TCK0: 8-bits timer clock source control bits.

TCK1	TCK0	Clock source of 8-bit timer (F_{TMR})
0	0	F_{CPU}
0	1	F_{SYS} (RTC, 32KHz)
1	0	TBOV (base timer overflow)
1	1	PA0 (port A)

BZEN: Buzzer output enable. (0:disable; 1:enable)

TEN: Timer counting enable. (0:disable; 1:enable)

✧ TMRL[010_H], Timer data low register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMR3	TMR2	TMR1	TMR0

TMR3~TMR0 are the low data of the 8-bits timer.

✧ TMRH[011_H], Timer data high register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMR7	TMR6	TMR5	TMR4

TMR7~TMR4 are the high data of the 8-bits timer.

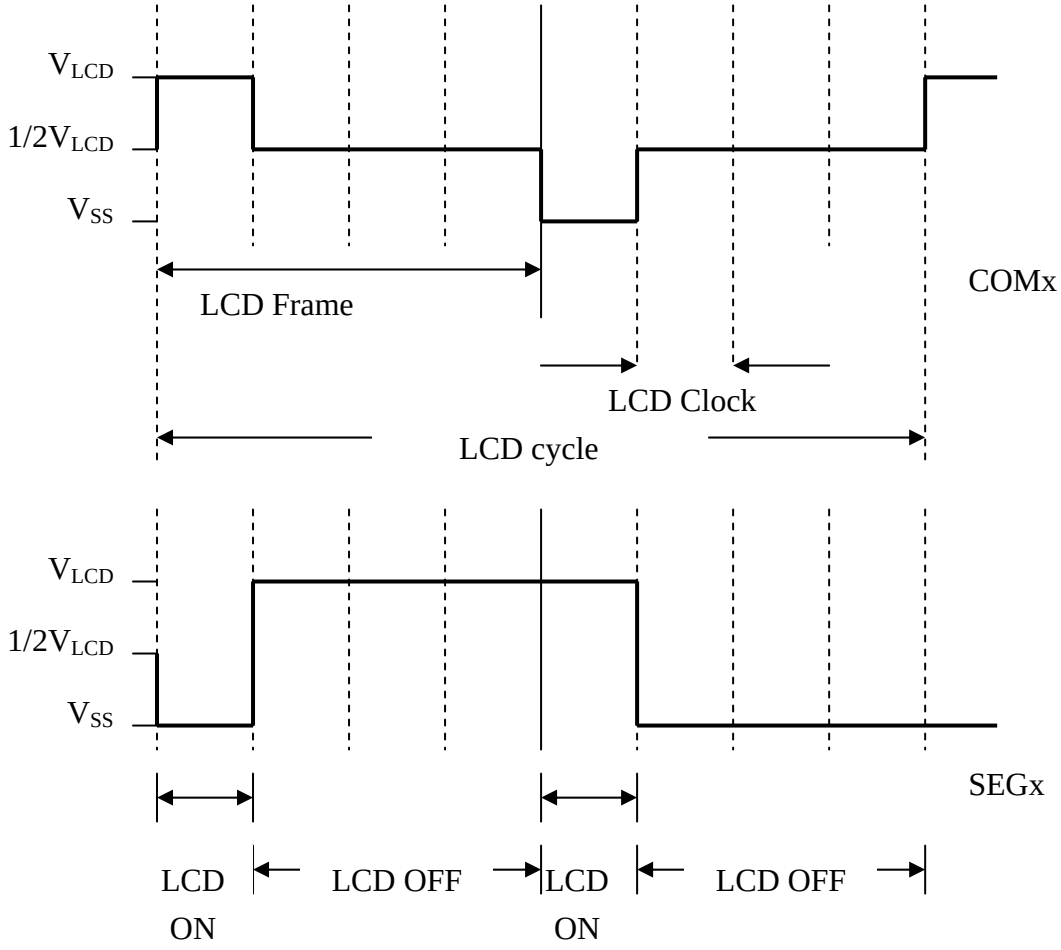
When the register is read, only the content of the timer/ counter be read; when the register is written, only writing into the pre-load register.

3. LCD

This chip can drive 48/39-dots LCD panel directly. The LCD driver contains controller, voltage generator, 4/3 common drivers, 12/13 segment drivers. There are 2 segment drivers (SEG12 & SEG11) are shared with general output ports (PB1 & PB0) optioned by mask. The 4 common or 3 common drivers are also selected by mask option. In the 3-common application, the COM3 driver has been changed to SEG0 driver.

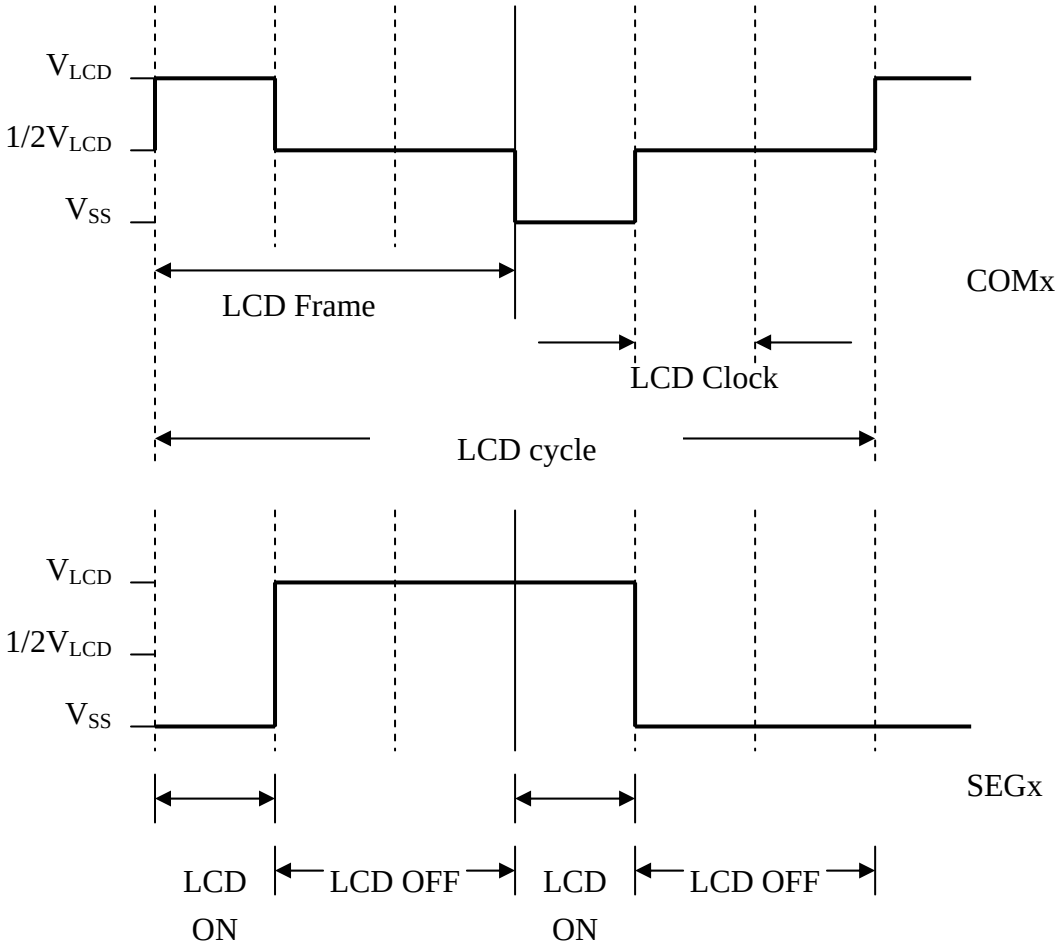
4-COM

LCD frame clock = 32KHz/(128*4)=64Hz



3-COM

LCD frame clock = 32KHz/(128*3)=85.3Hz



✧ LCDCN[012_H], LCD control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
-	-	-	LCDON

Bit3~Bit1: reserved, read as 0.

LCDON: LCD power control. (0: LCD power off, LCD no clock input; 1: LCD power on)

✧ LCD RAM Map

4-COM

	COM3	COM2	COM1	COM0
	Bit3	Bit2	Bit1	Bit0
013_H	**SEG0 (not used in 4-COM)**			
014_H	SEG1			
015_H	SEG2			
016_H	SEG3			
017_H	SEG4			
018_H	SEG5			
019_H	SEG6			
$01A_H$	SEG7			
$01B_H$	SEG8			
$01C_H$	SEG9			
$01D_H$	SEG10			
$01E_H$	SEG11			
$01F_H$	SEG12			

3-COM

	COM3	COM2	COM1	COM0
	Bit3	Bit2	Bit1	Bit0
013_H	Not used for 3-COM	SEG0		
014_H		SEG1		
015_H		SEG2		
016_H		SEG3		
017_H		SEG4		
018_H		SEG5		
019_H		SEG6		
$01A_H$		SEG7		
$01B_H$		SEG8		
$01C_H$		SEG9		
$01D_H$		SEG10		
$01E_H$		SEG11		
$01F_H$		SEG12		

4. Power saving mode (Stop mode & Sleep mode)

The CPU enters stop mode or sleep mode is operated by writing CPU power saving register PS [008_H]. During the power saving mode, CPU holds the internal status of the system. In stop mode, the F_{CPU} & F_{SYS} clock will be stopped and system need a warm-up time for the stability of system clock running after wake up.

✧ Power saving mode condition & Release

	Stop mode	Sleep mode
Internal RC (128K/32KHz)	Stopped	Stopped
RTC Crystal (32768Hz)	Stopped	Operated
CPU internal status	Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the executed address	
LCD	LCD display OFF	LCD display Retain
Timers	Stopped & Retain	Operated
Watchdog Timer	Clear WDT & Disable WDT	
Release Condition	RSTB, PA0INT, PA1INT, Keyboard wakeup	RSTB, PA0INT, PA1INT, TMRINT, BTINT, Keyboard Wakeup

✧ PS[008_H], CPU power saving register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
WDTEN	H/L	SLP	STP

WDTEN: Watchdog timer enable. (0:disable; 1:enable)

H/L: Internal RC frequency for T416 CPU selection bit. (0: 32KHz; 1: 128KHz)

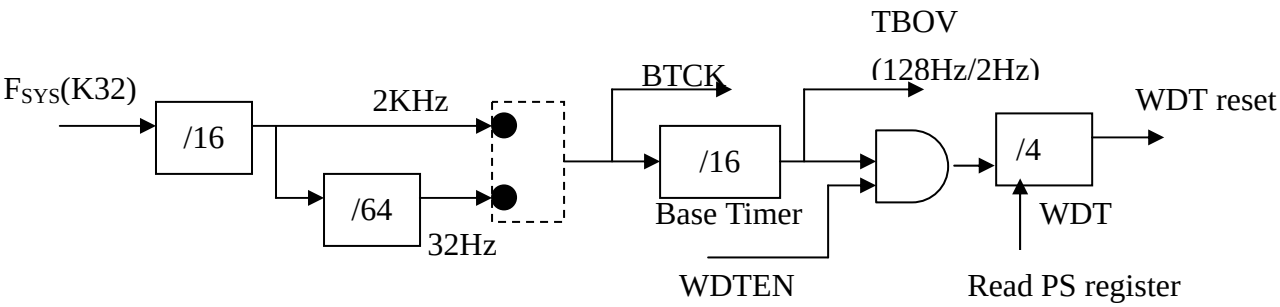
SLP: Into sleep mode. (0:inactive; 1:active)

STP: Into stop mode. (0:inactive; 1:active)

The SLP & STP bits will be cleared to “0” automatically, when the release conditions occur.

5. Watchdog timer

The watchdog timer frequency depends on the clock source of BTCK. That is the watch dog clock source is 2Hz or 128Hz optional by mask. The WDT can be enable or disabled by writing PS register. User can use the time up signal to prevent a software malfunction or sequence from jumping to an unknown location when system is fail. Normally, the watchdog time up signal initializes the chip reset under normal operation. The chip also provides clear watchdog command that is the programmer read PS register [008_H] can clear the watch dog timer only.



6. IO Port

There are total 4 general input ports (PA3~PA0), 2 general output ports (PB1~PB0) & 4 general I/O ports (PC3~PC0) in this chip. The PA3~PA0 can be defined as keyboard wake-up interrupt individually by mask option. All I/O ports (PC3~PC0) can be used for input & output operations under software control. The PC3~PC0 can be defined as keyboard wake-up interrupt individually by PCC & PC registers. The buzzer outputs are pins shared with PC1 (BZB) & PC0 (BZ). If the PC1 & PC0 set to be output mode and the BZEN bit in TMRC register set to "1", the buzzer function be enabled and the frequencies output selected by mask. The SEG12 & SEG11 (LCD segment drivers) are pins shared with PB1 (SEG12) & PB0 (SEG11), selected by mask option. If the LCD function of SEG12 & SEG11 be disabled, the PB1 & PB0 work as general output pins. Otherwise, SEG12/PB1 & SEG11/PB0 will be LCD segment drivers.

✧ PA [$00B_H$], Input port A register[R], default value [----]

Bit3	Bit2	Bit1	Bit0
PA3	PA2	PA1	PA0

PA3~PA0 are the data value of the Input port A.

When reading PA, the pads states are read.

✧ PB [$00C_H$], Output port B register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
-	-	PB1	PB0

PB1 & PB0 are the data value of the Output port B in O/P mode. (Port B can be selected as general O/P or LCD driver by mask.)

When reading PB, the data in PB registers are read.

✧ PCC [$00D_H$], I/O port C control register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PCC3	PCC2	PCC1	PCC0

PCC3~PCC0: PC3~PC0 I/O control bit. (0: output, 1: input)

✧ PC [$00E_H$], I/O port C register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PC3	PC2	PC1	PC0

PC3~PC0 are the data value of the I/O port C.

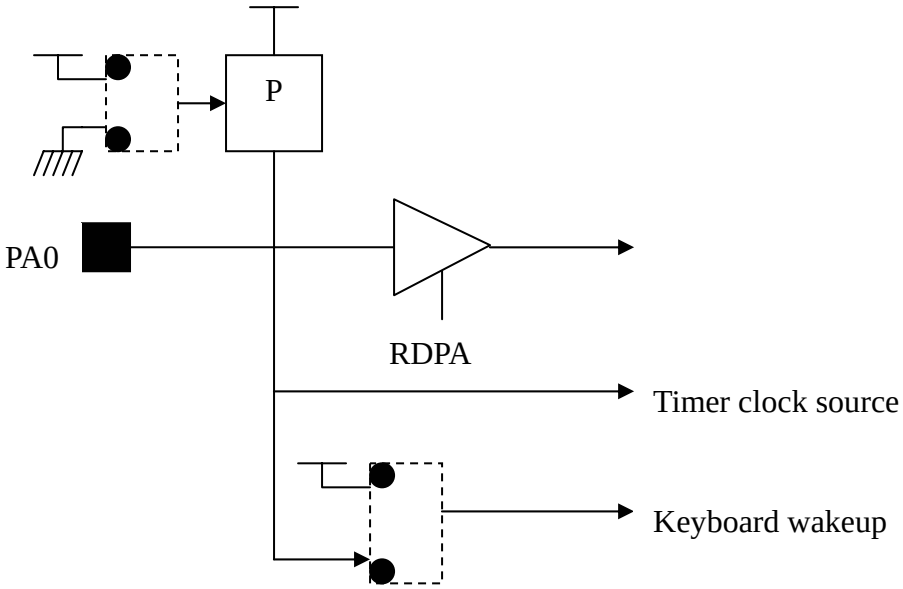
When writing PC, data are written into the PC registers.

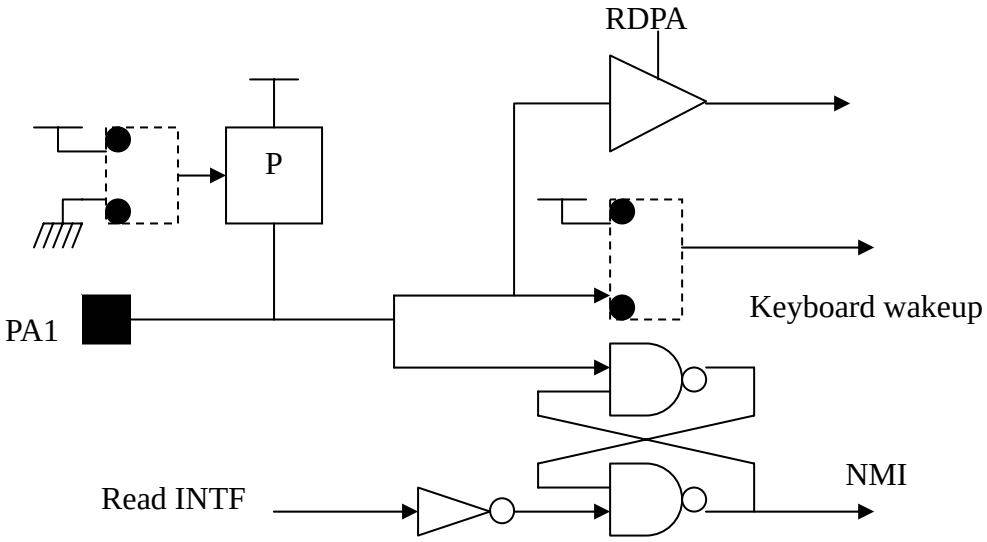
When reading PC & PC in input mode, the states in PC pads are read.

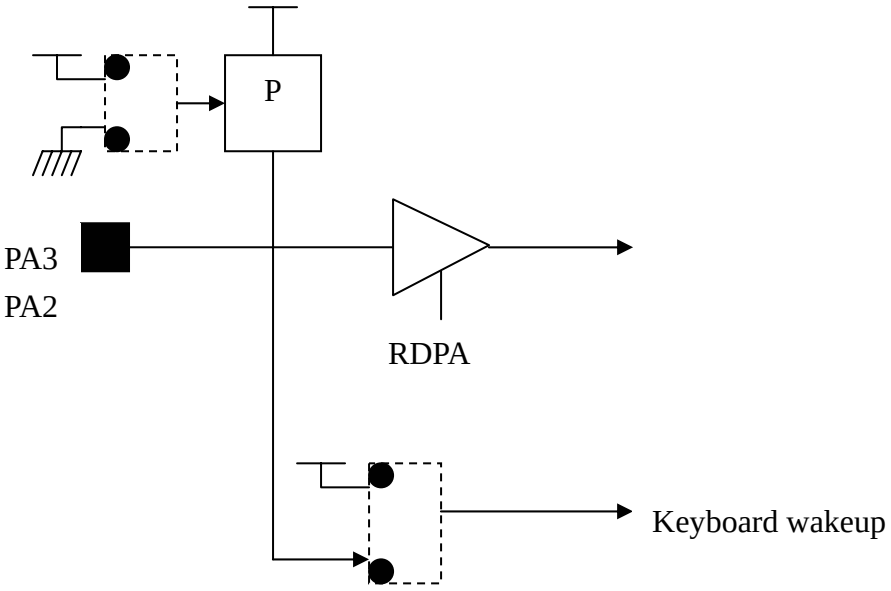
When reading PC & PC in output mode, the data in PC registers are read.

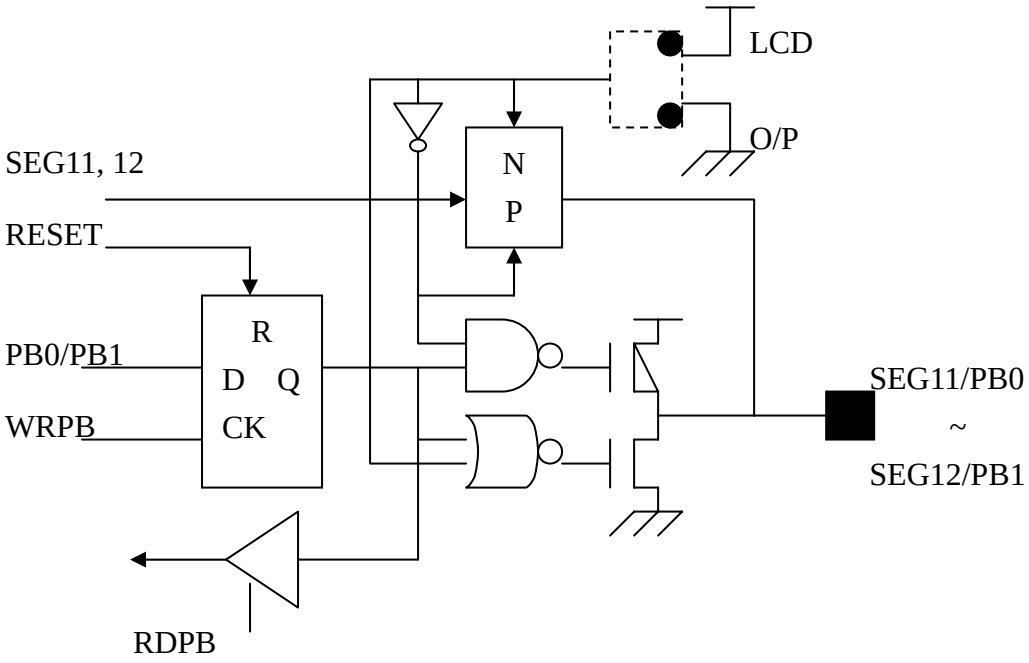
When the PC ports are set to input mode (PCCx=1), the PC register (PCx) be as the control bits to control the pull-high resistors enabled/disabled.

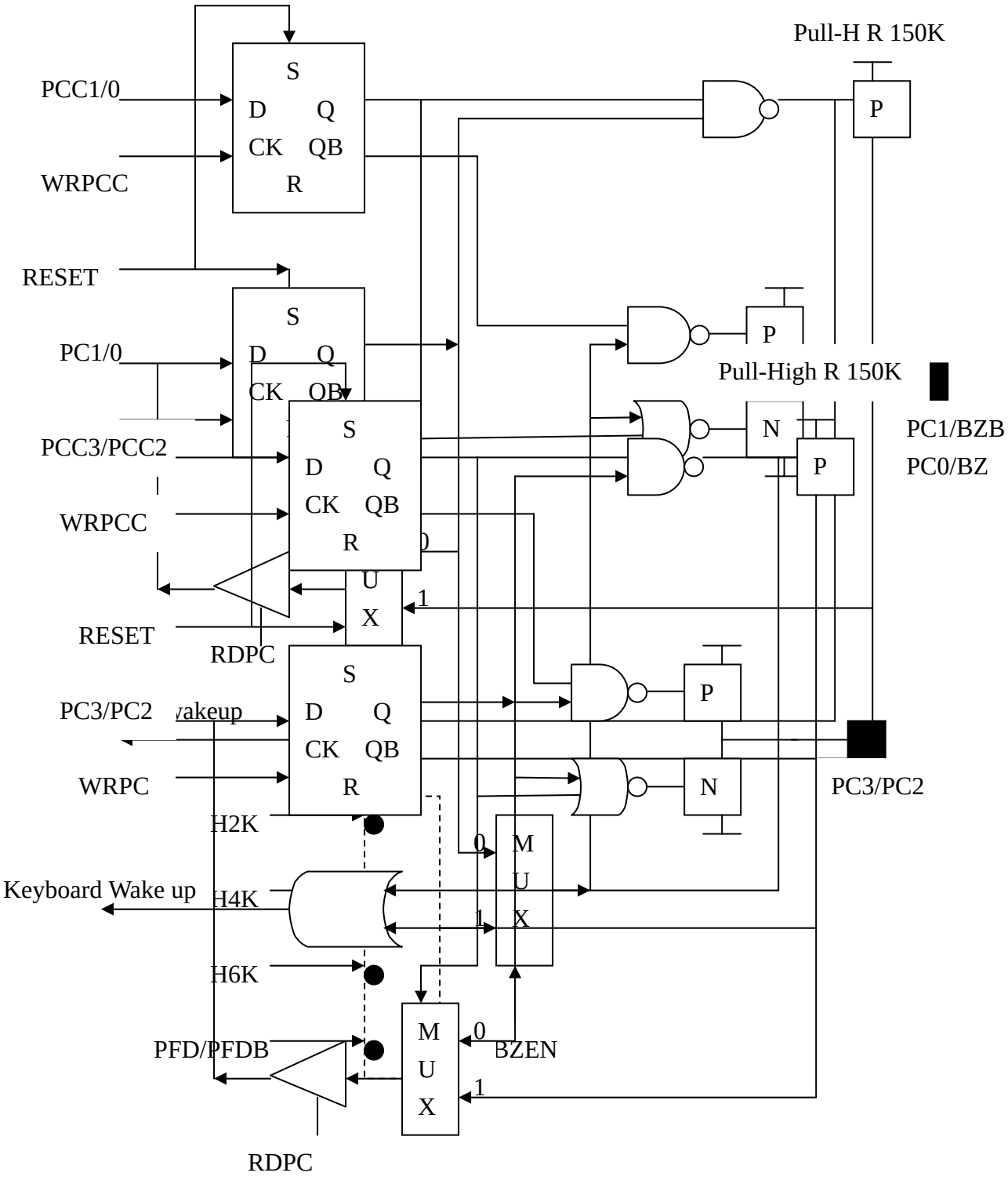
When the PCx & PCCx in PC & PCC registers are both set to "1", the corresponding PC port keyboard wakeup function will be enabled.


P
PA0
RDPA
Timer clock source
Keyboard wakeup


RDPA
P
PA1
Keyboard wakeup
Read INTF
NMI


P
PA3
PA2
RDPA
Keyboard wakeup


LCD
O/P
SEG11, 12
N
P
RESET
R
PB0/PB1
D Q
WRPB
CK
SEG11/PB0
~
SEG12/PB1
RDPB


Pull-H R 150K
PCC1/0
WRPCC
RESET
PC1/0
PCC3/PCC2
WRPCC
RESET
RDPC
PC3/PC2
WRPC
H2K
Keyboard Wake up
H4K
H6K
PFD/PFDB
RDPC
S
D Q
CK QB
R
P
N
Pull-High R 150K
PC1/BZB
PC0/BZ
PC3/PC2
M
U
X
BZEN
0
1

7. Interrupts

The chip provides total 4 interrupt sources. They are PA0 INT (PA0INT), PA1 INT (PA1INT), timer/counter INT (TINT) & base timer INT (BTINT). The interrupt control register INTC contains the interrupt control bits to enable and disable corresponding interrupt and the corresponding interrupt request flags in the INTF register.

If the interrupt needs service, the programmer may set the corresponding bit to allow interrupt nesting. PA0 & PA1 interrupts are triggered by a high to low transition and set the related interrupt request flags (FPA0 & FPA1). The internal timer/counter interrupt is initialized by setting FTMR to 1, resulting from the timer overflow. The base timer INT (BTINT) provides 2Hz or 128Hz interrupt optioned by mask.

When the corresponding interrupt enable bits are set to 1, the chip will active the interrupt service. If certain interrupt needs service, the corresponding service flag may set 1 to alert the interrupt service. Then CPU reads the service flag and proceeds with the interrupt service. After CPU reading the register, the service flag register INTF will be cleared to 0 to allow other interrupt requests happen during this interval.

✧ INTF [009_H], interrupt request flag register [R], default [0000]

Bit3	Bit2	Bit1	Bit0
FPA1	FPA0	FTMR	FBT

FPA1: PA1 interrupt request flag. (0:inactive; 1:active)

FPA0: PA0 interrupt request flag. (0:inactive; 1:active)

FTMR: Timer/counter interrupt request flag. (0:inactive; 1:active)

FBT: Base timer interrupt request flag. (0:inactive; 1:active)

✧ INTC [$00A_H$], interrupt control register [R/W], default [0000]

Bit3	Bit2	Bit1	Bit0
PA1IE	PA0IE	TMRIE	BTIE

PA1IE: Enable PA1 interrupt. (0:disable; 1:enable)

PA0IE: Enable PA0 interrupt. (0:disable; 1:enable)

TMRIE: Enable timer/counter interrupt. (0:disable; 1:enable)

BTIE: Enable base timer interrupt. (0:disable; 1:enable)

8. RESET

The chip has three kinds of reset source as follow

- POR (power on reset)
- External reset
- Watchdog timer reset

POR (power on reset)

The chip provides automatic reset function when the power is turned on.

External Reset (RSTB)

This is one kind of system resetting signal, but only operated device externally. When the chip acknowledged the low level from the pin RSTB, it will generate the reset signal to reset CPU & all the peripheral back to their initial state (default values).

Watchdog timer reset

This reset signal will generate automatically when the watchdog timer is enable. If the watchdog timer is disabled, no watchdog reset will occur. Normally, the watchdog time up signal initializes the chip reset under normal operation.

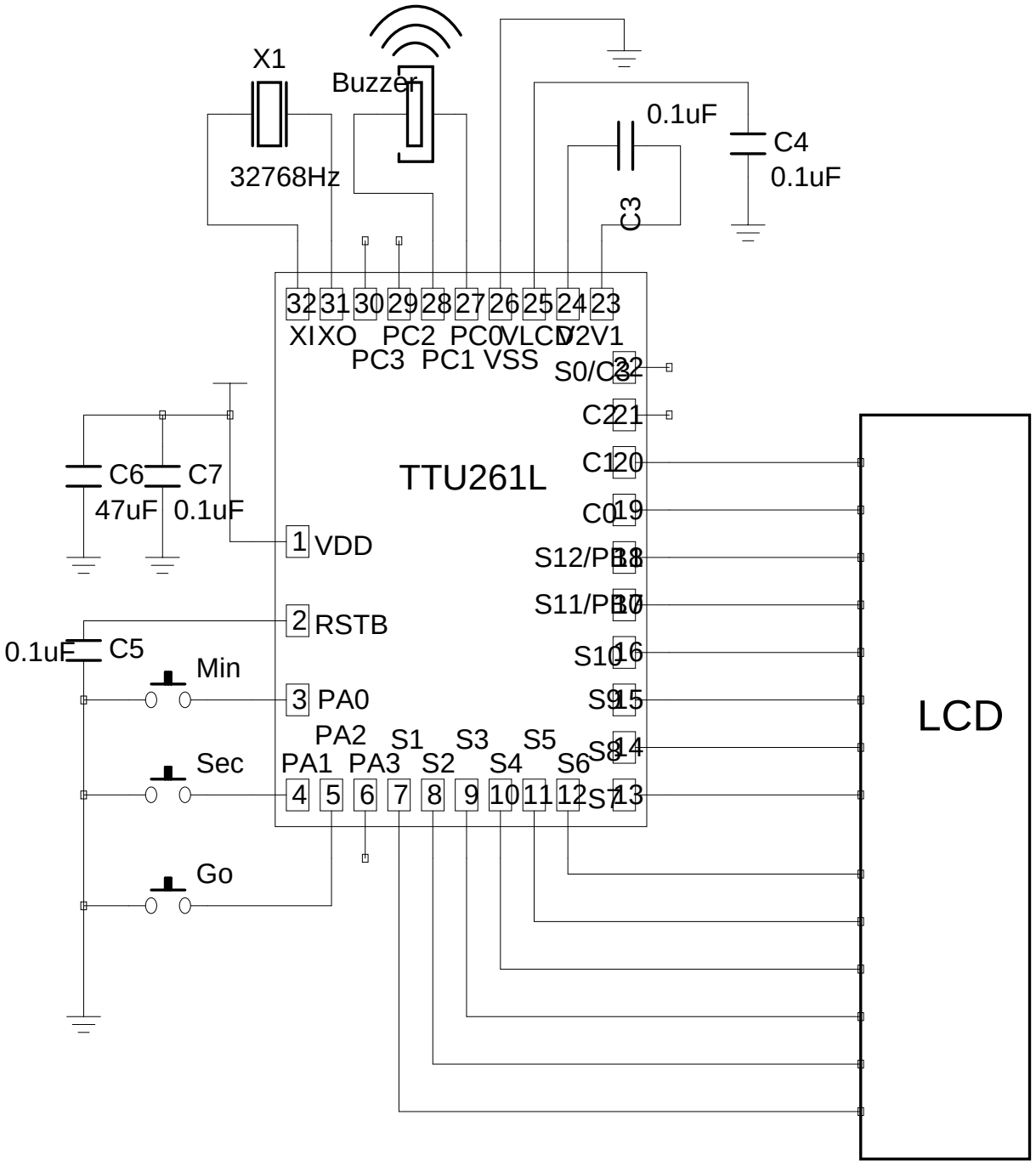
Mask Option Table:

The following table shows the mask option in this chip. All the mask options must define to ensure proper function.

Function	**Option**			
LCD type selection	4 common	3 common	-	-
Base Timer overflow frequency selection	128Hz	2Hz	-	-
PA0 selection	PHR & KBW	PHR & no KBW	No PHR & no KBW	-
PA1 selection	PHR & KBW	PHR & no KBW	No PHR & no KBW	-
PA2 selection	PHR & KBW	PHR & no KBW	No PHR & no KBW	-
PA3 selection	PHR & KBW	PHR & no KBW	No PHR & no KBW	-
PB0 selection	LCD	O/P	-	-
PB1 selection	LCD	O/P	-	-
Buzzer Frequency	PFD	2KHz	4KHz	6KHz

Note. PHR : pull-high resistor; KBW: keyboard wakeup

Application Circuit:



· Order Information :

a. Package form : TTU261L-zzz

b. Chip form : TCU261L-zzz

c. Wafer base : TDU261L-zzz