General Description:

TTU262L is an advanced 4-bit T416 microcontroller. It contains 4K-byte ROM, 256-nibble RAM, 16 I/O & 34*6 LCD (8 I/O pins share with LCD segment), which is designed for LCD products application. The device is suitable for application in family appliance, consumer product, particularly in timepiece application.

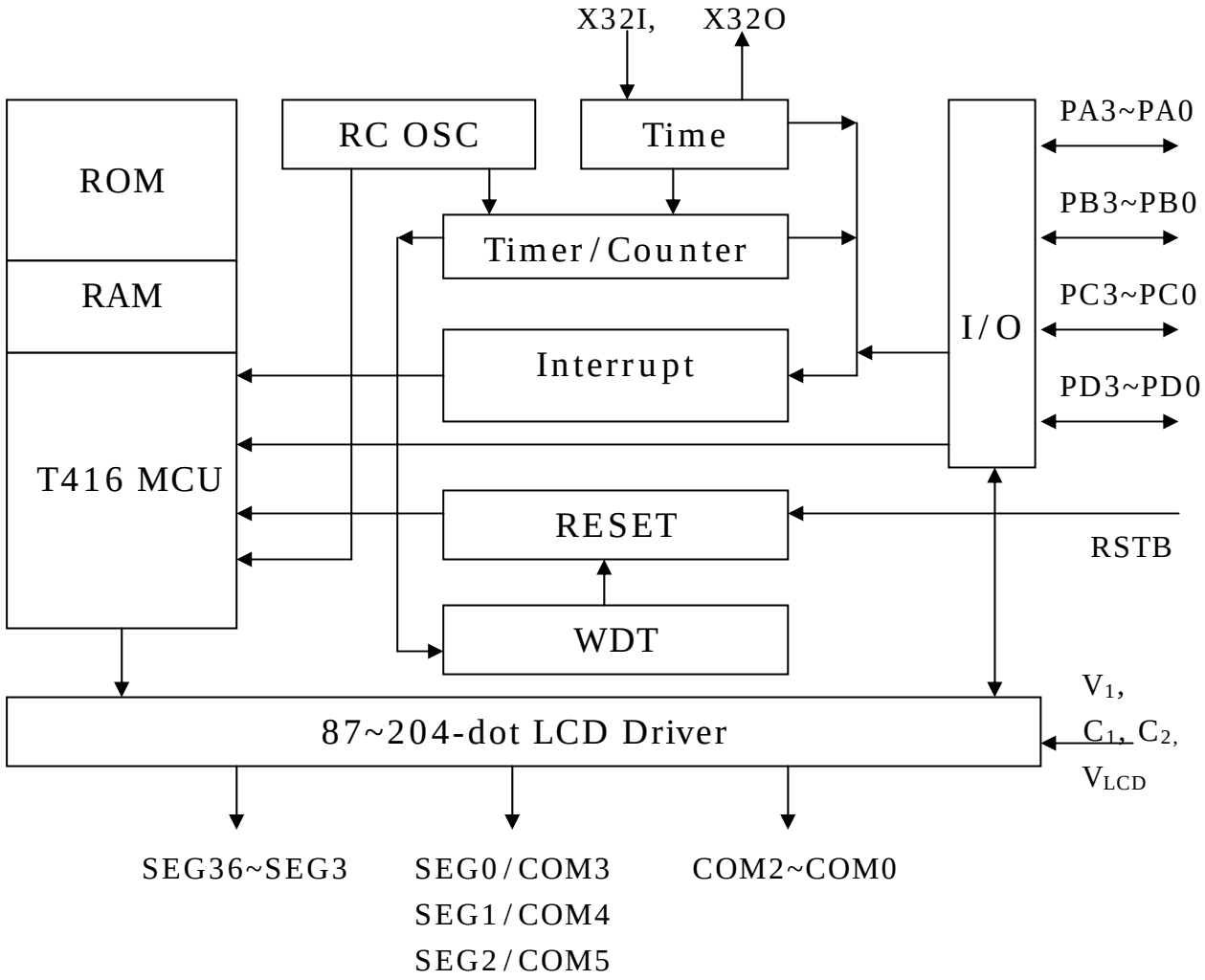
Features:

- ✧ 4-bit T416 MCU core
- ✧ 0.5um 1p2m CMOS process
- ✧ 4-level stack
- ✧ Operating voltage: 1.2V~1.8V
- ✧ Operating frequency:
  - ■ 128KHz/16KHz@1.5V
- ✧ Built-in 32768Hz crystal oscillator & internal RC oscillator
- ✧ 4K*16 program ROM
- ✧ 256*4 SRAM
- ✧ Max 16 general programming I/O pins
  - ■ Buzzer frequency selected by mask option
  - ■ PA1 & PA2 can be used as timer/counter inputs
  - ■ PC & PD ports share with LCD segment optioned by mask
- ✧ 87~204 dots C-type LCD display optioned by mask
  - ■ 6-COM, 5-COM, 4-COM or 3COM optioned by mask
  - ■ 1/3 bias or 1/2 bias selected by mask
  - ■ SEG29~SEG36 pins share with PC0~PC3 & PD0~PD3 optioned by mask
- ✧ Two 8-bit auto-reload timer/counter & one base timer
- ✧ Built-in software control for power saving function
- ✧ Built-in watch dog timer reset circuit
- ✧ Provides 4 interrupt sources
  - ■ External: PA0
  - ■ Internal: Timer/counter A, Timer/counter B, Base timer

Applications:

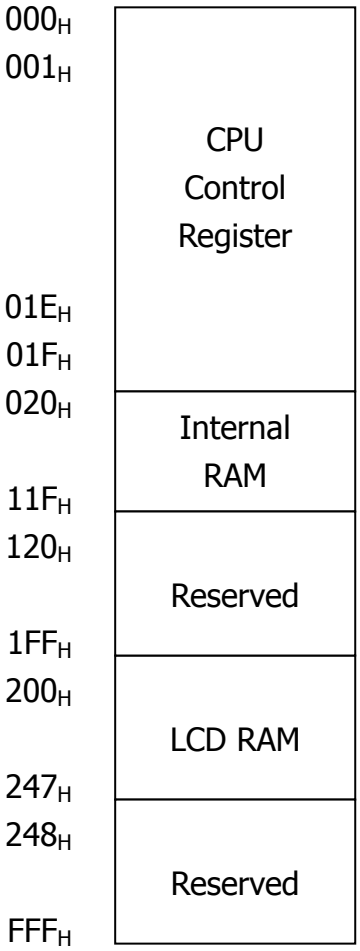
1. LCD products
2. Watch/ Timer
3. Counter/ Step counter/ Pedometer

Block Diagram:

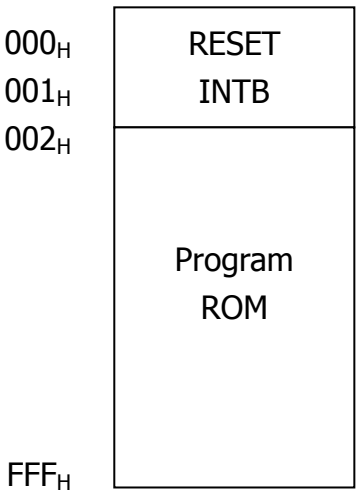


Functional Description:

Map of memory & I/O



Data Memory



Program Memory

Memory Map

000_H~FFF_H	Program ROM [4K*16]
000_H~$01F_H$	CPU control register
020_H~$11F_H$	Internal RAM [256*4]
200_H~247_H	LCD RAM [34*6 dots]

✧ **CPU Control Register**

Address	Symbol	R/W	Default	Description
000_H	DP1			
001_H	ACC			
002_H	TB0			
003_H	TB1			
004_H	TB2			
005_H	DPL			
006_H	DPM			
007_H	DPH			
008_H	PS	R/W	1000	CPU power saving register
009_H	INTF	R/W	0000	Interrupt request flag register
$00A_H$	INTC	R/W	0000	Interrupt control register
$00B_H$	PAC	R/W	1111	I/O port A control register
$00C_H$	PA	R/W	1111	I/O port A register
$00D_H$	PBC	R/W	1111	I/O port B control register
$00E_H$	PB	R/W	1111	I/O port B register
$00F_H$	PCC	R/W	1111	I/O port C control register
010_H	PC	R/W	1111	I/O port C register
011_H	PDC	R/W	1111	I/O port D control register
012_H	PD	R/W	1111	I/O port D register
013_H	TMAC	R/W	0000	Timer/counter A control register
014_H	TMAL	R/W	0000	Timer/counter A data low register
015_H	TMAH	R/W	0000	Timer/counter A data high register
016_H	TMBC	R/W	0000	Timer/counter B control register
017_H	TMBL	R/W	0000	Timer/counter B data low register
018_H	TMBH	R/W	0000	Timer/counter B data high register
019_H	FCR	R/W	0110	Function control register

1. Oscillators

✧ 32768 oscillator for system clock

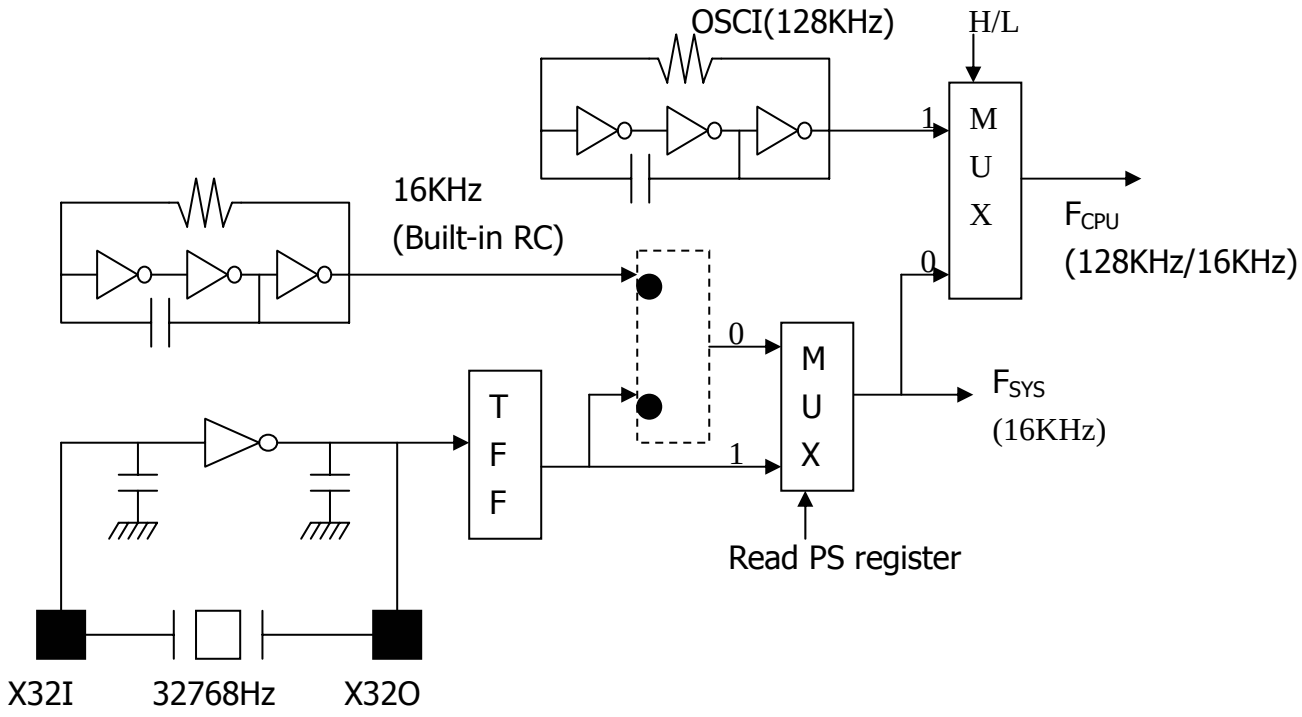
A 32768Hz crystal across X32I and X32O, no capacitors are connected between X32I/X32O and ground. The 32768Hz frequency divided by 2 has provided as peripheral system clock (F_{SYS}). Mask option determines whether the 32768Hz crystal is used or not.

✧ Internal RC oscillator (128KHz/16KHz)

The chip was built in an internal 128KHz/16KHz RC oscillator which is selected by H/L bit in PS register for T416 as CPU clock source. If the 32768Hz crystal is not used (disabled by mask option), the internal 16KHz RC oscillator was build as the peripheral system clock (F_{SYS}).

✧ System low speed mode (Built-in 16KHz RC oscillator or external 32KHz RTC)

The chip was built-in an internal 16KHz RC oscillator for low speed & low power consumption consideration. The low speed operation frequency comes from internal 16 KHz RC oscillator or external 32768Hz RTC (X32I & X32O) was selected by mask option. After power on reset, the low speed clock definitely stuck to internal RC oscillator (16KHz). The user can read the PS register to change the low speed clock source from internal RC to external RTC (32768Hz) divided by 2 constantly, if the external RTC selected by mask. We suggest reading the PS register after power on reset at least 1 second. The low speed clock source will eternalize change to external RTC after reading PS register until power on reset or wakeup from STOP mode.



2. Timer/Counter

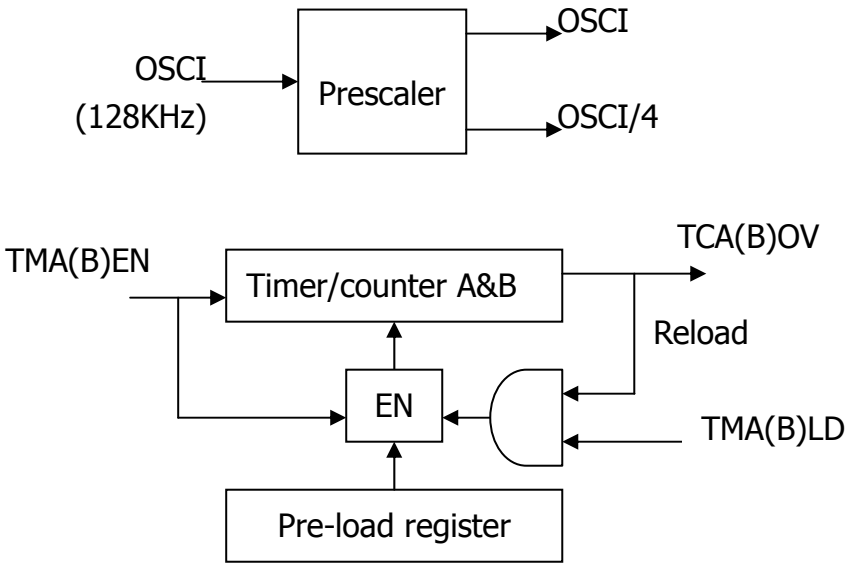
Two 8-bits timer/counters (TMRA & TMRB) with 4 clock sources each are implemented in this chip. The clock sources of TMRA & TMRB are defined by the timer control registers TMAC & TMBC.

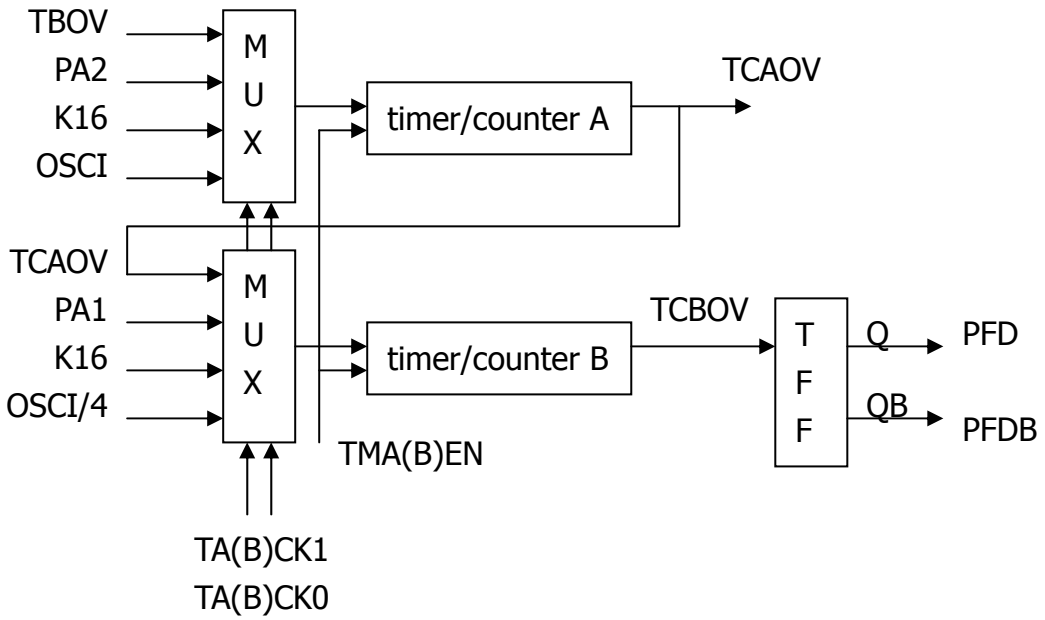
The timer/counter A & B can be cascaded to form a 16-bit timer/counter when the clock source of timer/counter B set to TCAOV. In the 16-bit timer application, "TMAEN" will enable the 16-bit timer/counter and TCBOV will reload the contents in the pre-load register into timer/counter, if the TMBLD is enabled.

Write TMA/BH(L) register only the data into pre-load register. The data in the pre-load register will be changed when writing TMA/BH(L). Writing TMA(B)C register bit0 "TMA(B)EN" to 1 to enable the timer/counter will auto-load the data in pre-load registers into timer/counter A(B) and start into counting.

Timer counts the current contents and generates an overflow flag. For example, the programmer writing "FE_H" into timer/counter will count 254 times timer clock and generate an overflow flag at the same time. The content "00_H" will count 256 clocks. When the overflow interrupt generates will reload the content in the pre-load register into timer, if the TMA(B)LD is enabled.

When the timer is counting, writing data will only keep into the pre-load register. The timer will still operate until overflow and then reload the new data into timer.





✧ TMAC[013_H], Timer/counter A control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMALD	TACK1	TACK0	TMAEN

TMALD: Timer/counter A auto-reload enable. (0:disable; 1:enable)

TACK1 & TACK0: Timer/counter A clock source selection bits.

TMAEN: Timer/counter A or 16-bit timer/counter counting enabled. (0:disable; 1:enable)

✧ TMBC[016_H], Timer/counter B control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMBLD	TBCK1	TBCK0	TMBEN

TMBLD: Timer/counter B or 16-bits timer/counter auto-reload enable. (0:disable; 1:enable)

TBCK1 & TBCK0: Timer/counter B clock source selection bits.

TMBEN: Timer/counter B counting enabled. (0:disable; 1:enable)

TA(B)CK1	TA(B)CK0	Timer A	Timer B
0	0	OSCI	OSCI/4
0	1	K16	K16
1	0	PA2	PA1
1	1	TBOV	TCAOV

TBOV: Time base overflow.

TCAOV: Timer/counter A overflow.

OSCI: comes from internal RC (128KHz). The OSCI (128KHz) clock will stop at the H/L bit in PS register reset to 0.

K16: 16KHz, comes from external 32KHz crystal or internal RC depends on the mask option.

✧ TMAL[014_H], Timer/counter A data low register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMA3	TMA2	TMA1	TMA0

TMA3~TMA0 are the low data of the timer/counter A.

✧ TMAH[015_H], Timer/counter A data high register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMA7	TMA6	TMA5	TMA4

TMA7~TMA4 are the high data of the timer/counter A.

✧ TMBL[017_H], Timer/counter B data low register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMB3	TMB2	TMB1	TMB0

TMB3~TMB0 are the low data of the timer/counter B.

✧ TMBH[018_H], Timer/counter B data high register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMB7	TMB6	TMB5	TMB4

TMB7~TMB4 are the high data of the timer/counter B.

When the register is read, only the content of the timer/counter be read; when the register is written, only writing into the pre-load register.

3. LCD

This chip can drive from 87 up to 204-dots C-type LCD panel directly. The LCD driver contains controller, voltage generator, 6~3 common drivers, 34~37 segment drivers. The 8 segment drivers (SEG36~SEG29) are shared with general I/O ports (PC & PD), optioned by mask. The LCD common driver can be selected as 6-COM, 5-COM, 4-COM or 3-COM by mask option. The 1/2 LCD bias or 1/3 bias also be selected by mask.

✧ FCR[019_H], Function control register[R/W], default value [0110]

Bit3	Bit2	Bit1	Bit0
BZEN	TBCK1	TBCK0	LCDON

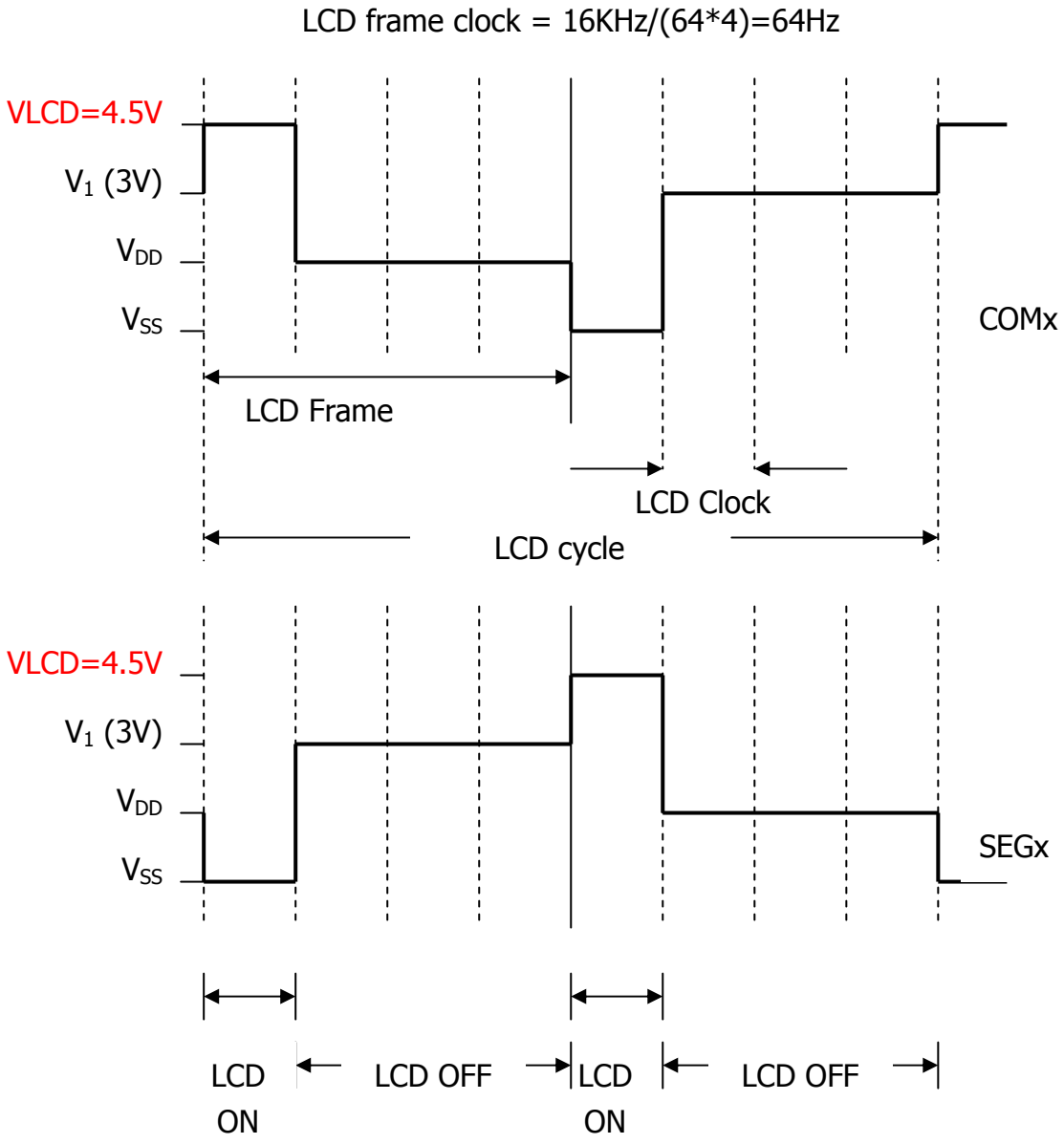
BZEN: Buzzer output enabled. (0:disable; 1:enable)

TBCK1 & TBCK0: Time base clock selection bits.

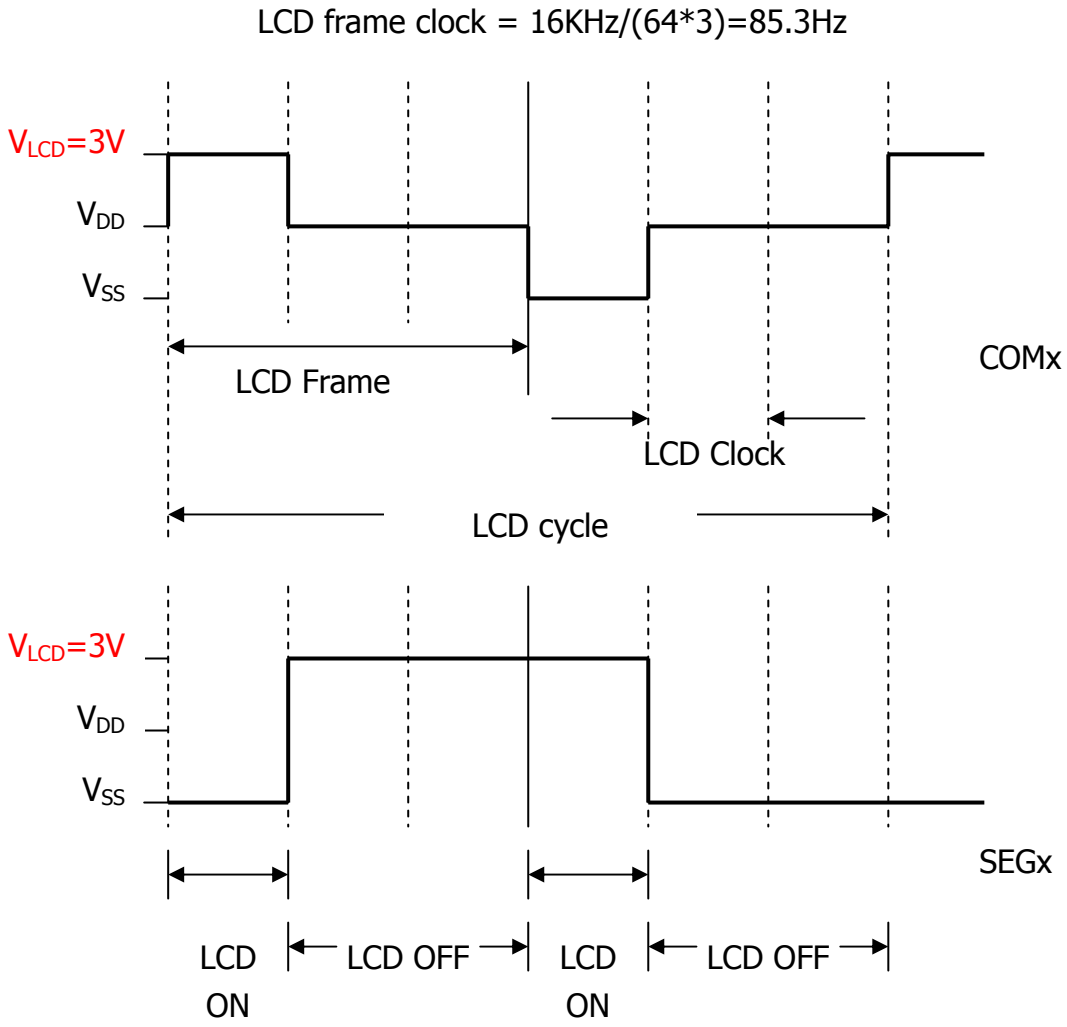
TBCK1	TBCK0	TBOV frequency
0	0	128Hz
0	1	32Hz
1	0	8Hz
1	1	2Hz

LCDON: LCD power control. (0: LCD power off, LCD no clock input; 1: LCD power on)

1/3 Bias, 4-COM


LCD frame clock = 16KHz/(64*4)=64Hz
VLCD=4.5V
V1 (3V)
VDD
VSS
COMx
LCD Frame
LCD Clock
LCD cycle
VLCD=4.5V
V1 (3V)
VDD
VSS
SEGx
LCD ON
LCD OFF
LCD ON
LCD OFF

1/2 Bias, 3-COM


LCD frame clock = 16KHz/(64*3)=85.3Hz
VLCD=3V
VDD
VSS
COMx
LCD Frame
LCD Clock
LCD cycle
VLCD=3V
VDD
VSS
SEGx
LCD ON
LCD OFF
LCD ON
LCD OFF

LCD RAM Map

3-COM

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	Reserved		COM5	COM4		COM3	COM2	COM1	COM0
225_H	NOT USED IN 3-COM				200_H	NOT USED IN 3-COM	SEG0		
226_H					201_H		SEG1		
227_H					202_H		SEG2		
228_H					203_H		SEG3		
229_H					204_H		SEG4		
$22A_H$					205_H		SEG5		
$22B_H$					206_H		SEG6		
$22C_H$					207_H		SEG7		
$22D_H$					208_H		SEG8		
$22E_H$					209_H		SEG9		
$22F_H$					$20A_H$		SEG10		
230_H					$20B_H$		SEG11		
231_H					$20C_H$		SEG12		
232_H					$20D_H$		SEG13		
233_H					$20E_H$		SEG14		
234_H					$20F_H$		SEG15		
235_H					210_H		SEG16		
236_H					211_H		SEG17		
237_H					212_H		SEG18		
238_H					213_H		SEG19		
239_H					214_H		SEG20		
$23A_H$					215_H		SEG21		
$23B_H$					216_H		SEG22		
$23C_H$					217_H		SEG23		
$23D_H$					218_H		SEG24		
$23E_H$					219_H		SEG25		
$23F_H$					$21A_H$		SEG26		
240_H					$21B_H$		SEG27		
241_H					$21C_H$		SEG28		
242_H					$21D_H$		SEG29		
243_H					$21E_H$		SEG30		
244_H					$21F_H$		SEG31		
245_H					220_H		SEG32		
246_H					221_H		SEG33		
247_H					222_H		SEG34		
					223_H		SEG35		
					224_H		SEG36		

4-COM

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	Reserved		COM5	COM4		COM3	COM2	COM1	COM0
225_H	NOT USED IN 4-COM				200_H	NOT USED IN 4-COM			
226_H					201_H	SEG1			
227_H					202_H	SEG2			
228_H					203_H	SEG3			
229_H					204_H	SEG4			
$22A_H$					205_H	SEG5			
$22B_H$					206_H	SEG6			
$22C_H$					207_H	SEG7			
$22D_H$					208_H	SEG8			
$22E_H$					209_H	SEG9			
$22F_H$					$20A_H$	SEG10			
230_H					$20B_H$	SEG11			
231_H					$20C_H$	SEG12			
232_H					$20D_H$	SEG13			
233_H					$20E_H$	SEG14			
234_H					$20F_H$	SEG15			
235_H					210_H	SEG16			
236_H					211_H	SEG17			
237_H					212_H	SEG18			
238_H					213_H	SEG19			
239_H					214_H	SEG20			
$23A_H$					215_H	SEG21			
$23B_H$					216_H	SEG22			
$23C_H$					217_H	SEG23			
$23D_H$					218_H	SEG24			
$23E_H$					219_H	SEG25			
$23F_H$					$21A_H$	SEG26			
240_H					$21B_H$	SEG27			
241_H					$21C_H$	SEG28			
242_H					$21D_H$	SEG29			
243_H					$21E_H$	SEG30			
244_H					$21F_H$	SEG31			
245_H					220_H	SEG32			
246_H					221_H	SEG33			
247_H					222_H	SEG34			
					223_H	SEG35			
					224_H	SEG36			

5-COM

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	Reserved		COM5	COM4		COM3	COM2	COM1	COM0
225_H	NOT USED IN 5-COM			SEG2	200_H	NOT USED IN 5-COM			
226_H				SEG3	201_H				
227_H				SEG4	202_H	SEG2			
228_H				SEG5	203_H	SEG3			
229_H				SEG6	204_H	SEG4			
$22A_H$				SEG7	205_H	SEG5			
$22B_H$				SEG8	206_H	SEG6			
$22C_H$				SEG9	207_H	SEG7			
$22D_H$				SEG10	208_H	SEG8			
$22E_H$				SEG11	209_H	SEG9			
$22F_H$				SEG12	$20A_H$	SEG10			
230_H				SEG13	$20B_H$	SEG11			
231_H				SEG14	$20C_H$	SEG12			
232_H				SEG15	$20D_H$	SEG13			
233_H				SEG16	$20E_H$	SEG14			
234_H				SEG17	$20F_H$	SEG15			
235_H				SEG18	210_H	SEG16			
236_H				SEG19	211_H	SEG17			
237_H				SEG20	212_H	SEG18			
238_H				SEG21	213_H	SEG19			
239_H				SEG22	214_H	SEG20			
$23A_H$				SEG23	215_H	SEG21			
$23B_H$				SEG24	216_H	SEG22			
$23C_H$				SEG25	217_H	SEG23			
$23D_H$				SEG26	218_H	SEG24			
$23E_H$				SEG27	219_H	SEG25			
$23F_H$				SEG28	$21A_H$	SEG26			
240_H				SEG29	$21B_H$	SEG27			
241_H				SEG30	$21C_H$	SEG28			
242_H				SEG31	$21D_H$	SEG29			
243_H				SEG32	$21E_H$	SEG30			
244_H				SEG33	$21F_H$	SEG31			
245_H				SEG34	220_H	SEG32			
246_H				SEG35	221_H	SEG33			
247_H				SEG36	222_H	SEG34			
					223_H	SEG35			
					224_H	SEG36			

6-COM

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	Reserved		COM5	COM4		COM3	COM2	COM1	COM0
225_H	NOT USED IN 6-COM				200_H	NOT USED IN 6-COM			
226_H	NOT USED IN 6-COM		SEG3		201_H				
227_H			SEG4		202_H				
228_H			SEG5		203_H	SEG3			
229_H			SEG6		204_H	SEG4			
$22A_H$			SEG7		205_H	SEG5			
$22B_H$			SEG8		206_H	SEG6			
$22C_H$			SEG9		207_H	SEG7			
$22D_H$			SEG10		208_H	SEG8			
$22E_H$			SEG11		209_H	SEG9			
$22F_H$			SEG12		$20A_H$	SEG10			
230_H			SEG13		$20B_H$	SEG11			
231_H			SEG14		$20C_H$	SEG12			
232_H			SEG15		$20D_H$	SEG13			
233_H			SEG16		$20E_H$	SEG14			
234_H			SEG17		$20F_H$	SEG15			
235_H			SEG18		210_H	SEG16			
236_H			SEG19		211_H	SEG17			
237_H			SEG20		212_H	SEG18			
238_H			SEG21		213_H	SEG19			
239_H			SEG22		214_H	SEG20			
$23A_H$			SEG23		215_H	SEG21			
$23B_H$			SEG24		216_H	SEG22			
$23C_H$			SEG25		217_H	SEG23			
$23D_H$			SEG26		218_H	SEG24			
$23E_H$			SEG27		219_H	SEG25			
$23F_H$			SEG28		$21A_H$	SEG26			
240_H			SEG29		$21B_H$	SEG27			
241_H			SEG30		$21C_H$	SEG28			
242_H			SEG31		$21D_H$	SEG29			
243_H			SEG32		$21E_H$	SEG30			
244_H			SEG33		$21F_H$	SEG31			
245_H			SEG34		220_H	SEG32			
246_H			SEG35		221_H	SEG33			
247_H			SEG36		222_H	SEG34			
					223_H	SEG35			
					224_H	SEG36			

4. Power saving mode (Stop mode & Sleep mode)

The CPU enters stop mode or sleep mode is operated by writing CPU power saving register PS [008_H]. During the power saving mode, CPU holds the internal status of the system. In stop mode, the F_{CPU} & F_{SYS} clock will be stopped and system need a warm-up time for the stability of system clock running after wake up.

✧ Power saving mode condition & Release

	Stop mode	Sleep mode
Internal RC Oscillator for CPU	Stopped	Stopped
External crystal 32KHz/Internal RC 16kHz	Stopped	Operated
CPU internal status	Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the executed address	
LCD	LCD display OFF	LCD display Retain
Timers	Stopped & Retain	Operated
Watchdog Timer (WDTEN)	Clear WDT counter	
Release Condition	RSTB, PA0INT, Keyboard wakeup	RSTB, PA0INT, TMAINT, TMBINT, BTINT, Keyboard Wakeup

*If the 32768Hz crystal is not connected, the peripheral system clock will be supported by internal RC oscillator in sleep mode.

✧ PS[008_H], CPU power saving register[R/W], default value [1000]

Bit3	Bit2	Bit1	Bit0
-	H/L	SLP	STP

Bit3: reserved, read as 1.

H/L: Internal RC frequency selection bit. (0: 16KHz; 1: 128KHz)

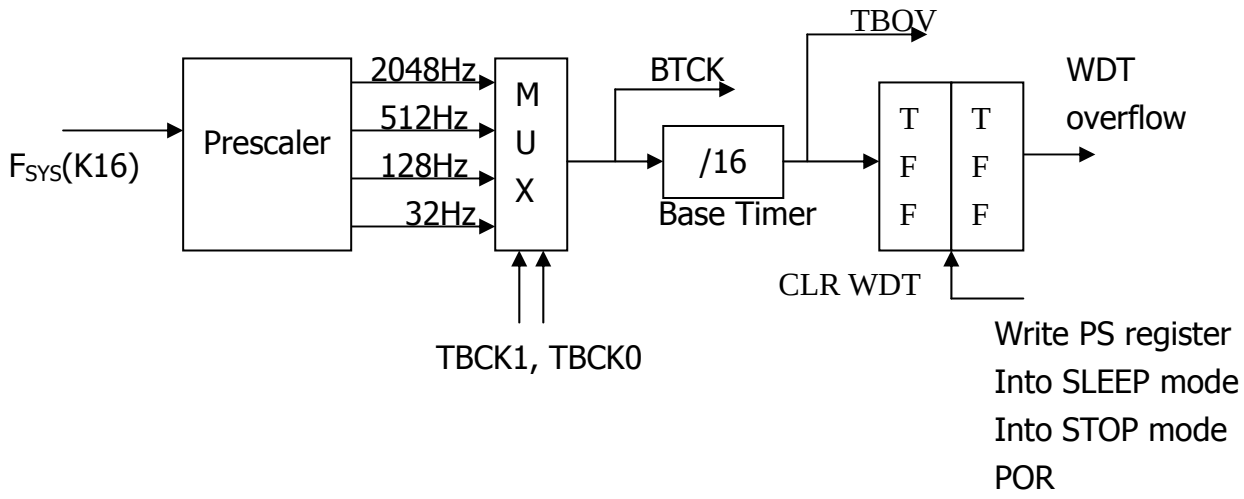
SLP: Into sleep mode. (0:inactive; 1:active)

STP: Into stop mode. (0:inactive; 1:active)

The SLP & STP bits will be cleared to "0" automatically, when the release conditions occur.

5. Watchdog timer

The watchdog timer frequency depends on the clock source of BTCK. That is the watch dog timer clock source is selected by programming FCR register. The watchdog timer is always enabled in this chip. After 4 TBOV clock raising edges, the chip will generate the watchdog overflow signal. User can use the time up signal to prevent a software malfunction or sequence from jumping to an unknown location when system is fail. Normally, the watchdog time up signal initializes the chip reset under normal operation. The chip also provides clear watchdog command that is the programmer writes any data to PS register [008_H] can clear the watchdog timer counter only. Of course the WDT counter also be cleared and stopped, if the chip into sleep mode or stop mode.



✧ FCR[019_H], Function control register[R/W], default value [0110]

Bit3	Bit2	Bit1	Bit0
BZEN	TBCK1	TBCK0	LCDON

BZEN: Buzzer output enabled. (0:disable; 1:enable)

TBCK1 & TBCK0: Time base clock selection bits.

TBCK1	TBCK0	TBOV frequency
0	0	128Hz
0	1	32Hz
1	0	8Hz
1	1	2Hz

LCDON: LCD power control. (0: LCD power off, LCD no clock input; 1: LCD power on)

6. IO Port

There are total 16 general I/O ports (PA3~PA0, PB3~PB0, PC3~PC0 & PD3~PD0) in this chip. The PA0 can be defined as external interrupt by programming INTC register. All I/O ports can be used for input & output operations under software control. The I/O ports can be defined as keyboard wake-up function individually by programming control & data registers. The buzzer output BZB/BZ is pin shared with PB0/PB1. If the PB0/PB1 set to be output mode and the BZEN bit in FCR register set to "1", the buzzer function be enabled and the frequencies output selected by mask. The SEG36~SEG29 (LCD segment drivers) are pins shared with PC3~PC0 & PD3~PD0, selected by mask option. If the LCD function be disabled, the PC port & PD port work as general I/O pins and keyboard wakeup function enabled. Otherwise, the pins will be LCD segment drivers and disabled keyboard wakeup function automatically.

✧ PAC [$00B_H$], I/O port A control register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PAC3	PAC2	PAC1	PAC0

PAC3~PAC0: PA3~PA0 I/O control bit. (0: output, 1: input)

✧ PA [$00C_H$], I/O port A register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PA3	PA2	PA1	PA0

PA3~PA0 are the data value of the I/O port A.

✧ PBC [$00D_H$], I/O port B control register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PBC3	PBC2	PBC1	PBC0

PBC3~PBC0: PB3~PB0 I/O control bit. (0: output, 1: input)

✧ PB [$00E_H$], I/O port B register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PB3	PB2	PB1	PB0

PB3~PB0 are the data value of the I/O port B.

✧ PCC [$00F_H$], I/O port C control register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PCC3	PCC2	PCC1	PCC0

PCC3~PCC0: PC3~PC0 I/O control bit. (0: output, 1: input)

✧ PC [010_H], I/O port C register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PC3	PC2	PC1	PC0

PC3~PC0 are the data value of the I/O port C.

✧ PDC [011_H], I/O port D control register[R/W], default value [1111]

Bit3	Bit2	Bit1	Bit0
PDC3	PDC2	PDC1	PDC0

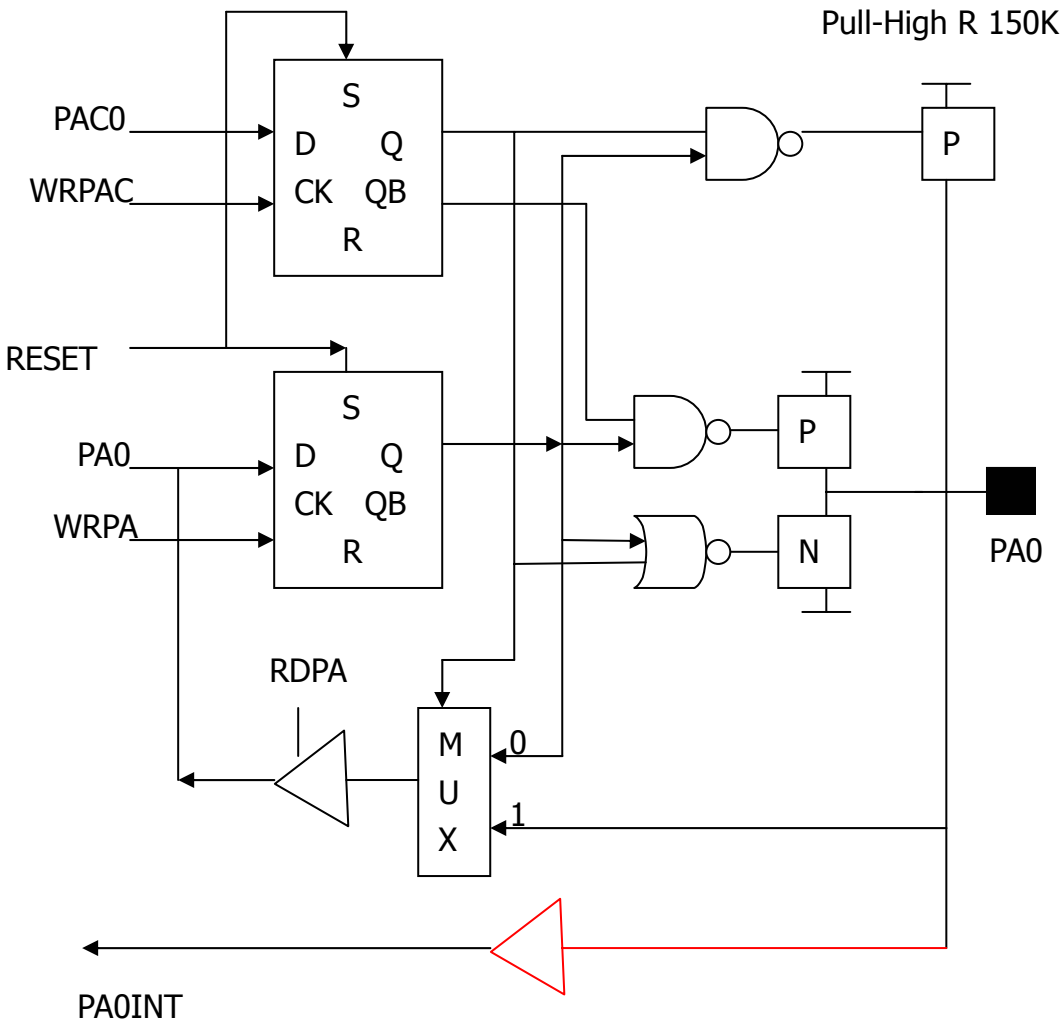
PDC3~PDC0: PD3~PD0 I/O control bit. (0: output, 1: input)

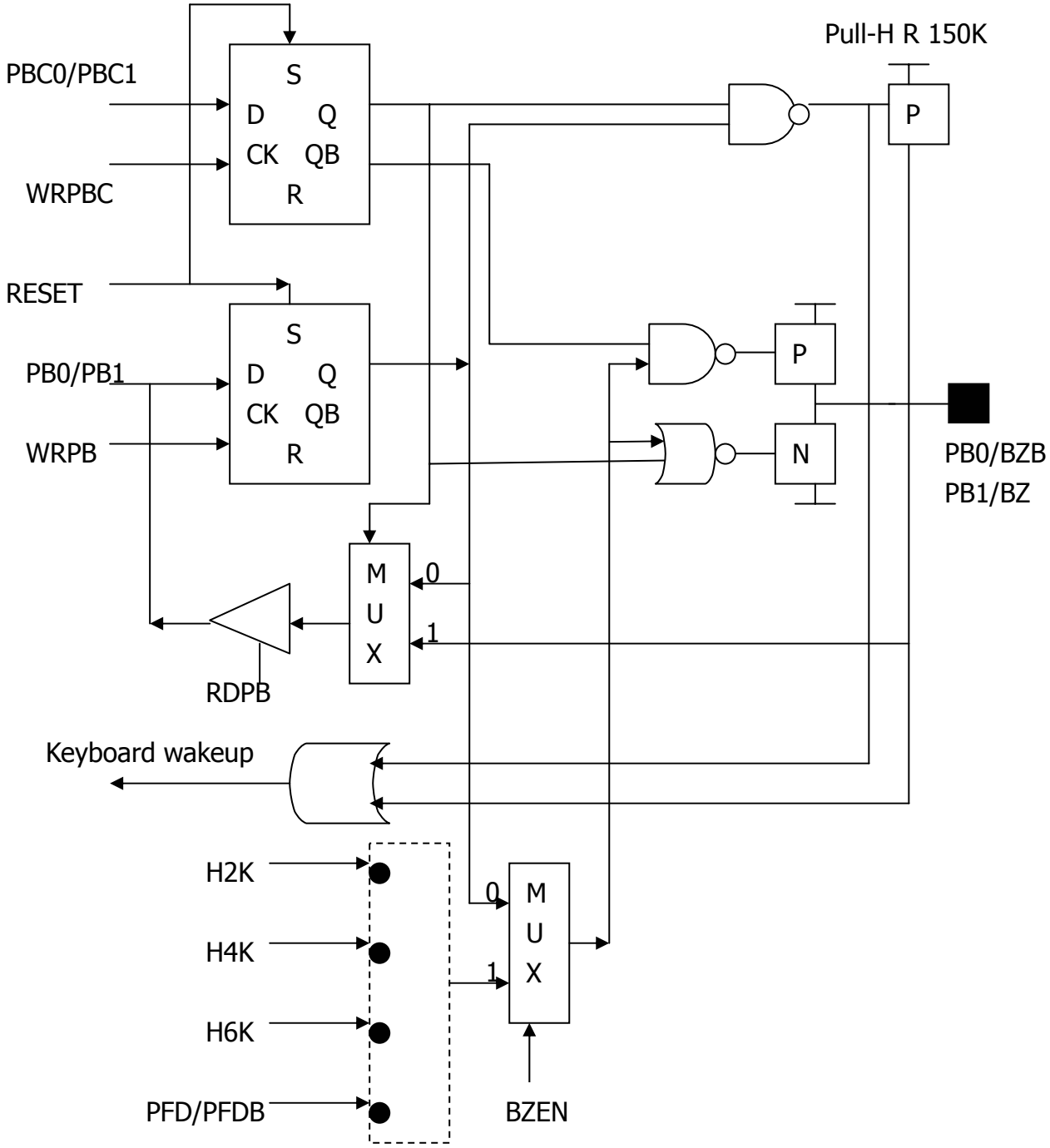
✧ PD [012_H], I/O port D register[R/W], default value [1111]

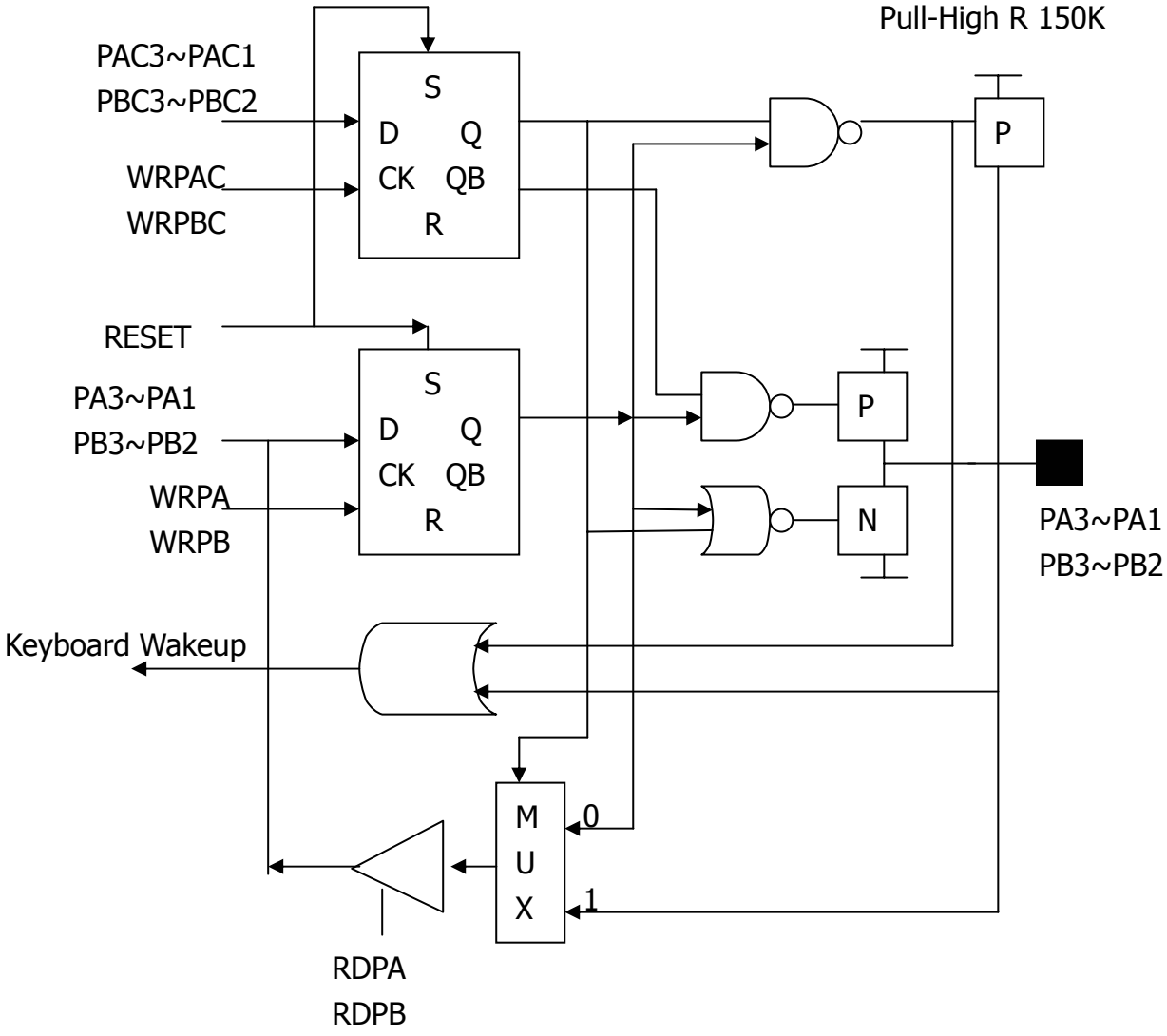
Bit3	Bit2	Bit1	Bit0
PD3	PD2	PD1	PD0

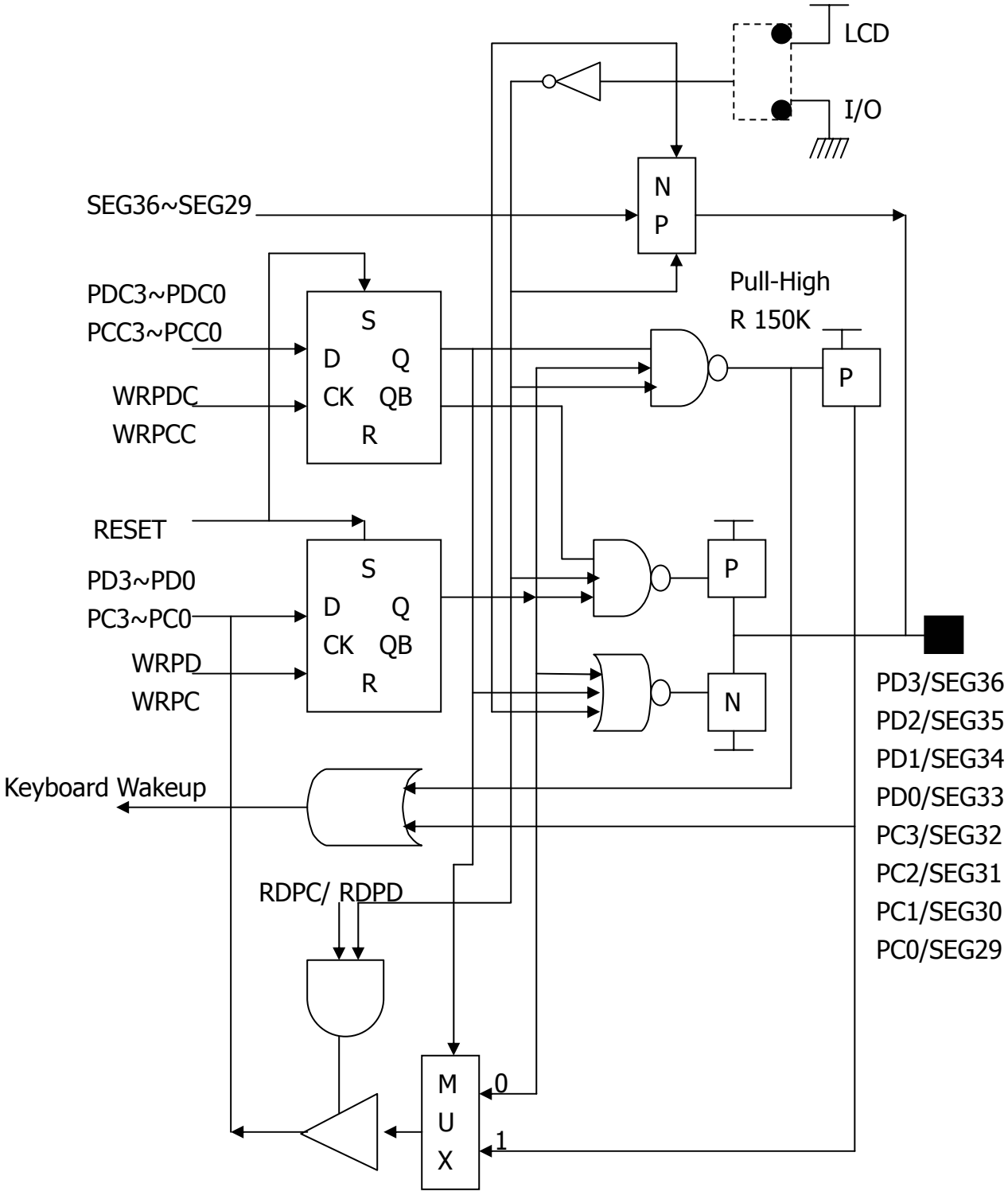
PD3~PD0 are the data value of the I/O port D.

When writing PA (PB, PC, PD) data are written into the PA (PB, PC, PD) registers.
When reading PA (PB, PC, PD) & PA (PB, PC, PD) in input mode, the states in PA (PB, PC, PD) pads are read.
When reading PA (PB, PC, PD) & PA (PB, PC, PD) in output mode, the data in PA (PB, PC, PD) registers are read.
When the PA (PB, PC, PD) ports are set to input mode, the PA (PB, PC, PD) register be as the control bits to control the pull-high resistors enabled/disabled.
When the PAx (PBx, PCx, PDx) & PACx (PBCx, PCCx, PDCx) in PA (PB, PC, PD) & PAC (PBC, PCC, PDC) registers are both set to "1", the corresponding PA (PB, PC, PD) port keyboard wakeup function will be enabled.




Pull-H R 150K
PBC0/PBC1
WRPBC
RESET
PB0/PB1
WRPB
S
D Q
CK QB
R
P
N
PB0/BZB
PB1/BZ
M
U
X
0
1
RDPB
Keyboard wakeup
H2K
H4K
H6K
PFD/PFDB
BZEN


Pull-High R 150K
PAC3~PAC1
PBC3~PBC2
WRPAC
WRPBC
S
D Q
CK QB
R
P
RESET
PA3~PA1
PB3~PB2
WRPA
WRPB
S
D Q
CK QB
R
P
N
PA3~PA1
PB3~PB2
Keyboard Wakeup
M
U
X
0
1
RDPA
RDPB


LCD
I/O
N
P
SEG36~SEG29
PDC3~PDC0
PCC3~PCC0
WRPDC
WRPCC
S
D Q
CK QB
R
Pull-High
R 150K
P
RESET
PD3~PD0
PC3~PC0
WRPD
WRPC
S
D Q
CK QB
R
P
N
PD3/SEG36
PD2/SEG35
PD1/SEG34
PD0/SEG33
PC3/SEG32
PC2/SEG31
PC1/SEG30
PC0/SEG29
Keyboard Wakeup
RDPC/ RDPD
M
U
X
0
1

7. Interrupts

The chip provides total 4 interrupt sources. They are PA0INT (PA0INT), timer/counter A INT (TMAINT), timer/counter B INT (TMBINT) & base timer INT (BTINT). The interrupt control register INTC contains the interrupt control bits to enable and disable corresponding interrupt and the corresponding interrupt request flags in the INTF register.

If the interrupt needs service, the programmer may set the corresponding bit to allow interrupt nesting. The PA0INT was triggered by a high to low transition at PA0, when the interrupt occurs the related interrupt request flag (FPA0) will be set. The internal timer/counter A or B interrupt is initialized by setting FTMA or FTMB to 1, resulting from the timer overflow. The base timer INT (BTINT) provides 128Hz, 32Hz, 8Hz and 2Hz interrupt optioned by programming FCR register.

When the corresponding interrupt enable bits are set to 1, the chip will active the interrupt service. If certain interrupt needs service, the corresponding service flag may set 1 to alert the interrupt service. Then CPU reads the service flag and proceeds with the interrupt service. After CPU writes the corresponding bits to 0 in the INTF register, the service flag will be cleared to 0 to allow other interrupt requests happen; the CPU writes "1" in the INTF register will not change the corresponding data in the register.

✧ INTF [009_H], interrupt request flag register [R/W], default [0000]

Bit3	Bit2	Bit1	Bit0
FPA0	FTMA	FTMB	FBT

FPA0: PA0 interrupt request flag. (0:inactive; 1:active)

FTMA: Timer/counter A interrupt request flag. (0:inactive; 1:active)

FTMB: Timer/counter B interrupt request flag. (0:inactive; 1:active)

FBT: Base timer interrupt request flag. (0:inactive; 1:active)

✧ INTC [$00A_H$], interrupt control register [R/W], default [0000]

Bit3	Bit2	Bit1	Bit0
PA0IE	TMAIE	TMBIE	BTIE

PA0IE: Enable PA0 interrupt. (0:disable; 1:enable)

TMAIE: Enable timer/counter A interrupt. (0:disable; 1:enable)

TMBIE: Enable timer/counter B interrupt. (0:disable; 1:enable)

BTIE: Enable base timer interrupt. (0:disable; 1:enable)

8. RESET

The chip has three kinds of reset source as follow

- POR (power on reset)
- External reset
- Watchdog timer reset

POR (power on reset)

The chip provides automatic reset function when the power is turned on.

External Reset (RSTB)

This is one kind of system resetting signal, but only operated device externally. When the chip acknowledged the low level from the pin RSTB, it will generate the reset signal to reset CPU & all the peripheral back to their initial state (default values).

Watchdog timer reset

The watchdog timer is always enabled in this chip. The reset signal will generate automatically when the watchdog timer is overflow. Normally, the watchdog time up signal initializes the chip reset under normal operation.

Mask Option Table:

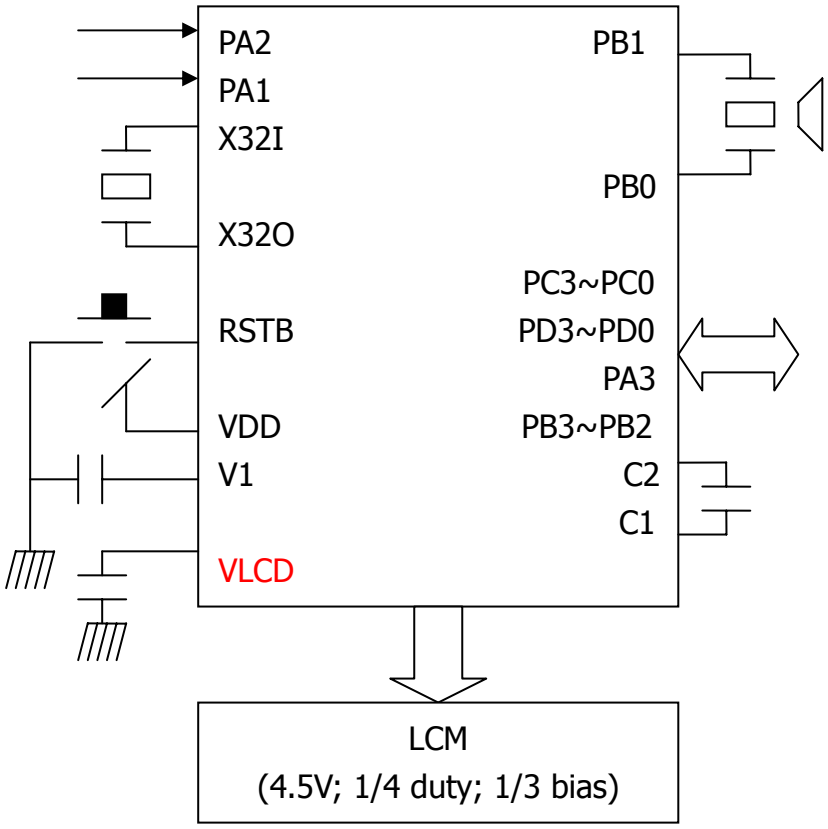
The following table shows the mask option in this chip. All the mask options must define to ensure proper function.

Function selection	Option Bit	Features
RTC OSC	0	32768 HZ crystal OSC
	1	16K RC OSC
Common of LCD	00	3 com
	01	4 com
	10	5 com
	11	6 com
LCD bias	0	1/2 bias
	1	1/3 bias
PD0~PD3 & PC0~PC3 IO port Or SEG36~SEG29 LCD Segment	0xxx	SEG36~SEG29 enable
	1000	SEG35~SEG29 enable, PD3 enable
	1001	SEG34~SEG29 enable, PD3~PD2 enable
	1010	SEG33~SEG29 enable, PD3~PD1 enable
	1011	SEG32~SEG29 enable, PD3~PD0 enable
	1100	SEG31~SEG29 enable, PD3~PD0 & PC3 enable
	1101	SEG30~SEG29 enable, PD3~PD0 & PC3~PC2 enable
	1110	SEG29~SEG29 enable, PD3~PD0 & PC3~PC1 enable
	1111	SEG36~SEG29 disable, PD3~PD0 & PC3~PC0 enable
Buzzer output	00	PFD
	01	2KHz
	10	4KHz
	11	6KHz

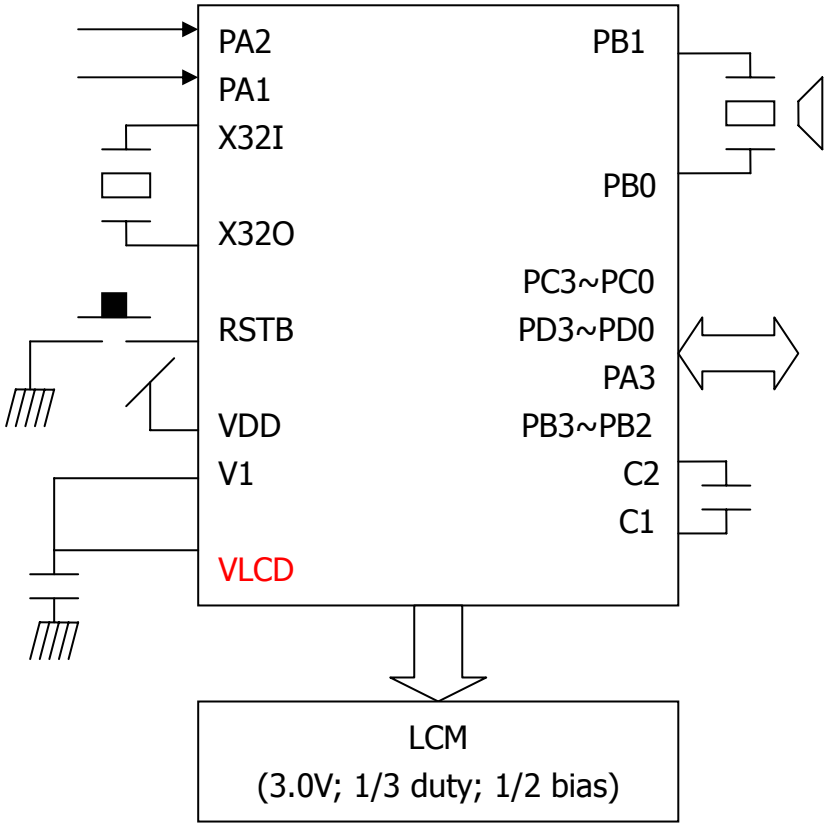
Pin Description:

Pin Name	I/O	Description
V_{DD}		Positive power supply
V_{SS}		Negative power supply, ground
X32I	I	32768Hz crystal input, can be connected to crystal, resistor or floating
X32O	O	32768Hz crystal output, can be connected to crystal, resistor or floating
PA3~PA0	I/O	Bidirectional 4-bits I/O port, PA2 & PA1 can be used as timer/counter A & B clock sources. PA0 can be defined as external interrupt. PA3 ~ PA1 used as general I/O pins.
PB3~PB2, PB1/BZ PB0/BZB	I/O	Bidirectional 4-bits I/O port, PB1 & PB0 can be used as buzzer output or general I/O port. PB3 ~ PB2 used as general I/O pins.
PC3/SEG32, PC2/SEG31, PC1/SEG30, PC0/SEG29,	I/O	Bidirectional 4-bits I/O port, LCD segment driver outputs or general I/O ports, determined by mask option
PD3/SEG36, PD2/SEG35, PD1/SEG34, PD0/SEG33,	I/O	Bidirectional 4-bits I/O port, LCD segment driver outputs or general I/O ports, determined by mask option
SEG28~SEG3	O	Segment drivers for LCD display
COM3/SEG0 COM4/SEG1 COM5/SEG2	O	Common driver (COM3, COM4, COM5) or segment driver (SEG0, SEG1, SEG2) for LCD display selected by mask option.
COM2~COM0	O	Common drivers for LCD display
V_1, C_1, C_2, V_{LCD}		LCD voltage & LCD voltage pump (C-type LCD) V_1, V_{LCD}, can be connected with external resistors to adjust LCD voltage in R-type LCD (SU262, SR262)
RSTB	I	External reset input, active low, internal pull-high resistor

Application Circuit:



TTU262L C-type LCD



TTU262L C-type LCD

DC Characteristics: (V_{DD}=1.5V, Ta=25°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	F_{OSC}=128KHz	1.2	1.5	1.8	V
Operating Current (normal mode)	I_{dd1}	F_{OSC}=128KHz, I/O no load, LCD on	-	35	-	uA
	I_{dd2}	F_{OSC}=16KHz, I/O no load, LCD on	-	20	-	
Operating Current (sleep mode)	I_{dd3}	I/O no load, LCD on	-	2	3	
Standby Current	I_{STB}	I/O no load, F_{CPU} & F_{SYS} stop	-	-	1.0	uA
PA, PB, PC, PD Input Low Voltage	V_{IL}		0	-	0.2	V_{DD}
PA, PB, PC, PD Input High Voltage	V_{IH}		0.8	-	1.0	V_{DD}
PA, PB, PC, PD Sink Current	I_{OL}	V_{DD}=1.5V, V_{OL}=0.5V	1.0	2.0	-	mA
PA, PB, PC, PD Source Current	I_{OH}	V_{DD}=1.5V, V_{OH}=1.0V	-1.0	-2.0	-	mA
PA, PB, PC, PD, RSTB Pull-High R	R_{PH}	V_{DD}=1.5V	100	150	200	KΩ
Oscillator Start up voltage	V_{ST}	32KHz crystal	1.4	-	-	V
Oscillator Sustain voltage	V_{SU}	32KHz crystal	1.2	-	-	V

AC Characteristics:

Parameter	Test Condition		Min	Typ	Max	Unit
Oscillator Frequency	F_{OSC}	V_{DD}=1.5V	-	128	-	KHz
System Frequency	F_{SYS}	V_{DD}=1.5V	-	16	-	KHz
System Startup Period	T_{OSC1} (128KHz/16KHz)	Power-up	-	RESET+4	-	F_{OSCL}
	T_{OSC2} (128KHz/16KHz)	wake-up from SLEEP mode or STOP mode	-	4	-	
System Stable Period	RC from 128KHz to 16KHz		-	4	-	F_{OSCL}
	RC from 16KHz to 128KHz		-	4	-	

Pin Assignment: