

A/D MCU

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General Description

The MCU provides cost effective for ADC application。 It designs by LSI high technology with low power process。

Features

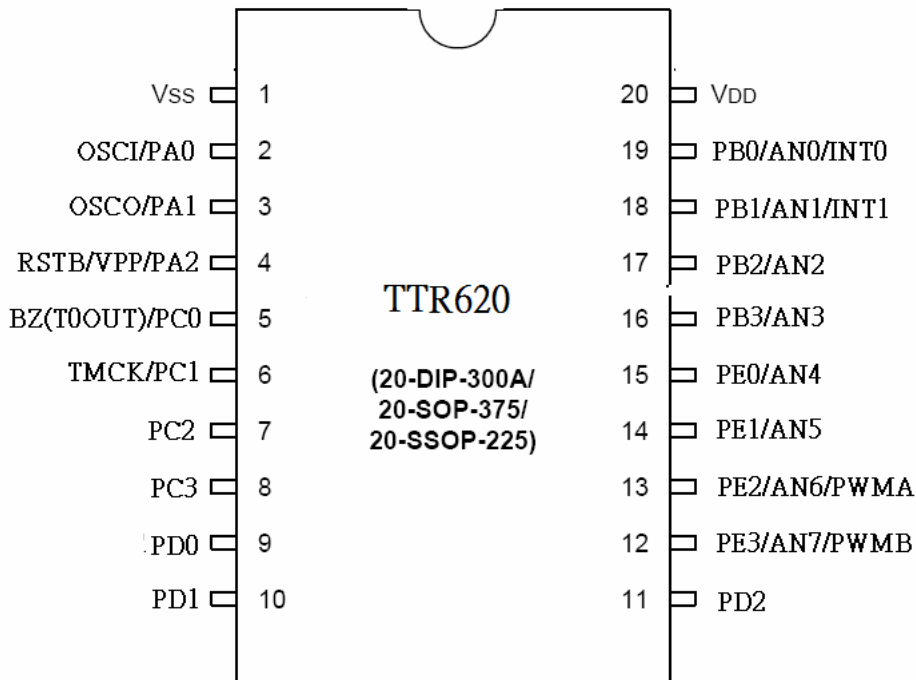
- ✧ Use 4-bit CPU core
- ✧ Operating Voltage :
 - (TTR620)OTP type : 2.2v-5.5v (fsys=4Mhz), 3.3v-5.5v (fsys=8Mhz)
- ✧ Oscillator type (Mask Option)
 - Resonator oscillator 1M-8Mhz(external capacitor)
 - Built-in RC oscillator external resistor, internal capacitor (400K-4Mhz)
 - **Internal RC oscillator : (4Mhz)**
 - **I/O define**
 - External clock input(OSCH)
 - Internal RC oscillator 16Khz
- ✧ ROM 4K*16, RAM 256*4
- ✧ Built-in 4 stacks
- ✧ Built-in a time base with internal interrupt
- ✧ Built-in watch dog timer
- ✧ Built-in Programming frequency divider function for buzzer function
- ✧ Stop function and sleep function feature to reduce power consumption
- ✧ **Built-in 1 set 8-bit Timer/counter with auto-reload**
- ✧ Built-in 2 set 8-bit PWM
- ✧ Low voltage reset function
- ✧ Built-in 8 bits ADC 8 channels (with internal interrupt function, conversion time is 64us @4Mhz) (8-bit resolution)
- ✧ **Max 17 I/O ports , 1 Input port .**
- ✧ Provide external reset pin and internal reset pin
- ✧ Provide 20/16 -pin SDIP/SOP

Application

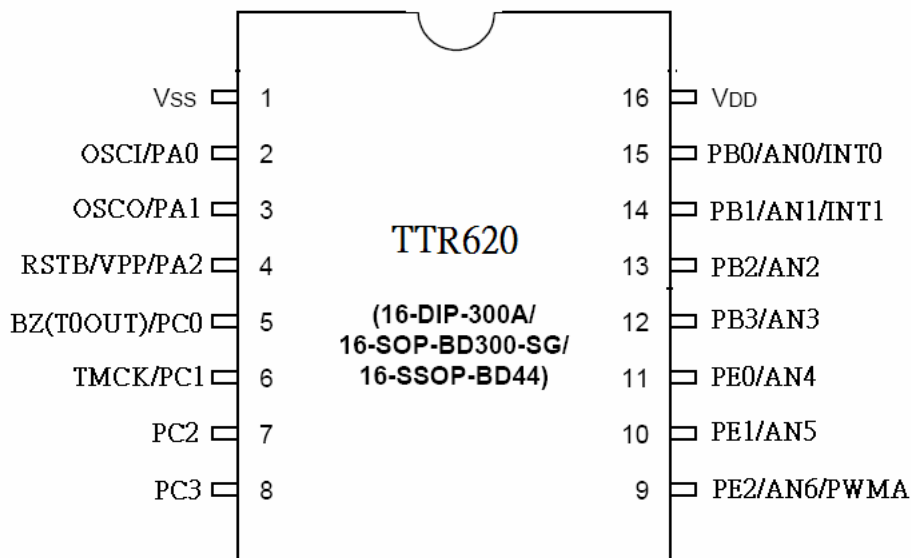
- Electric appliances controller
- Consumer products
- Toy controller

.Pin Assignment

20 PIN



16 PIN



.Pin Description

Name	I/O	Description
VSS	P	Digital ground pin
AVSS	P	Analog ground pin
PA0/OSCI	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). there can be selected as oscillator pin : Crystal mode : crystal input , External RC mode : RC oscillator input , External clock input .
PA1/ OSCO	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). there can be selected as oscillator pin : Crystal mode : crystal output , External RC mode : Oscillator frequency divided by 2 is available on OSCO to synchronize other logic or used for testing purpose.
PA2/RSTB/VPP	I	General purpose I port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). there can be selected as reset pin , with pull high 50Kohm @5v .
PC0/BZ	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). Ther can be selected as buzzer function select by software programming.
PC1/TMCK	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, there can be selected as external wake-up function or external clock input for Timer/Counter1 circuit .
PC2	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger).
PC3	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger).
PD0	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger).
PD1	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger).
PD2	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger).
PE3/AN7/PWMA	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically. Ther can be selected as PWM function select by software programming
PE2/AN6/PWMB	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically. Ther can be selected as PWM function select by software programming
PE1/AN5	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). There can be selected as an A/D input, the I/O function and pull-high

		resistor are disabled automatically.
PE0/AN4	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically.
PB3/AN3	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically.
PB2/AN2	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger). There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically.
PB1/AN1/INT1	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software. There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically. there can be selected as external interrupt input function
PB0/AN0/INT0	I/O	General purpose I/O port, hysteresis input, pull high 150Kohm @5v selected by software. There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically. there can be selected as external interrupt input function
AVDD	P	Analog power pin
VDD	P	Digital power pin

Note – Please notice input pin pull high or output pin driving current capacity in this table.

AC / DC Characteristics

Absolutely max. ratings

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20°C - +70°C	°C
Storage Temperature	Tsto	-50°C - +125°C	°C
Supply Voltage	VDD	6.0	V
Voltage to input terminal	Vin	Vss-0.3 to Vdd+0.3	V

D.C. Characteristics

(Condition : Ta= 25 ± 3 °C, RH ≤ 65 %, VDD = + 3V, VSS=0V)

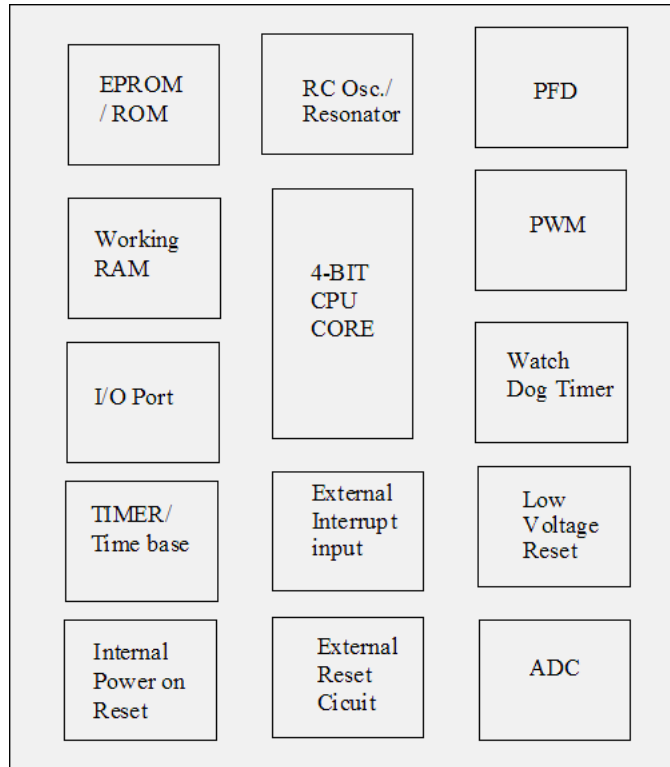
Item	Symbol	Condition	min.	typ.	Max.	unit
Operating voltage	VDD1	Fsys=4Mhz	2.2	3.0	5.5	V
Operating voltage	VDD2	Fsys=8Mhz	3.3	5.0	5.5	V
Power consumption current	IOPR1	System clock at 8Mhz resonator, No load, @5.0V, ADC off		4.0	8.0	mA
Power consumption current	IOPR2	System clock at 4Mhz resonator, No load, @5.0V, ADC off		2.5	5.0	mA
Power consumption current	IOPR3	System clock at 4Mhz RC oscillator, No load, @5.0V, ADC off		2.5	5.0	mA
Power consumption current	IOPR4	System clock at 32Khz crystal oscillator, No load, @3.0V, ADC off		20	40	uA
ADC power consumption	IAD1	Additional power consumption when ADC use(ADC clock is 1Mhz and VDD=3V)		0.5	1	mA
ADC power consumption	IAD2	Additional power consumption when ADC use(ADC clock is 1Mhz and VDD=5V)		1.5	3	mA
Halt current	Ist2	System halt, No load @3.0V, WDT disable			1	uA
Input low voltage for input and I/O port	VIL1		0		0.3VDD	V
Input high voltage for input and I/O port	VIH1		0.7VDD		VDD	V
Input low voltage for RESB pin	VIL2		0		0.4VDD	V
Input high voltage for RESB pin	VIH2		0.9VDD		VDD	V
I/O port sink current	IOL1	VOL=0.1VDD, @5.0V	4	8	16	mA
I/O port source current	IOH1	VOH=0.9VDD, @5.0V	2	4	8	mA

Pull high resistance	R_{UP}	@5V	100	150	200	Kohm
Resonator oscillator sustain voltage	V_{SU}		2.1			V
LVR current	I_{LVR}	@ 3.0V		70	100	uA
A/D input voltage	V_{ADI}	(Vref=VDD)	0		VDD	V
A/D conversion error	E_{ADC}	When VDD from 2.7V-5.5V		±0.5		LSB

.A.C. Characteristics

Item	Symbol	Condition	min.	typ.	Max.	unit
System clock1	f_{SYS1}	Resonator oscillator @3.0v		4		MHz
System clock2	f_{SYS2}	RC oscillator @3.0v, external resistor		4		MHz
Watch dog clock	f_{WDT}	(internal oscillator circuit) @3v 25°C	8	16	32	Khz
External reset low pulse width	t_{RES}		1			us
ADC conversion time	t_{ADC}	At 4Mhz system clock, ADC clock is 1MHZ		64		us

.Block Diagram



Function Description

1 : Map of memory and I/Os

000H	(DP1)
001H	A
002H	TB1
003H	TB2
004H	TB3
005H	DPL
006H	DPM
007H	DPH
008H	PS
009H	INTF
00AH	INTC
00BH	Edge&LVR
00CH	PAC
00DH	PA
00EH	PBC
00FH	PB
010H	PCC
011H	PC
012H	PDC
013H	PD
014H	PEC
015H	PE
016H	TBC/BZC
017H	TMR1L
018H	TMR1H
019H	TMR1C
01AH	PWM1DL
01BH	PWM1DH
01CH	ADL
01DH	ADH
01EH	ADCTL0
01FH	ADCTL1
020H	RAM
11FH	PWMC
120H	AD-SEL0
121H	AD-SEL1
122H	
123H	
124H	PWM2DL
125H	PWM2DH
126H	
127H	
128H	
129H	
12AH	PWMCK
FFFH	Reserved

Data memory map

000	Reset vector
001	INTB vector
002	
	On-chip program memory
FFF	

Program memory map

2: I/O MAP TABLE

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
000H	Index					0000
		R/W	R/W	R/W	R/W	
001H	ACC	ACC3	ACC2	ACC1	ACC0	0000
		R/W	R/W	R/W	R/W	
002H	TB1	D7	D6	D5	D4	0000
		R/W	R/W	R/W	R/W	
003H	TB2	D11	D10	D9	D8	0000
		R/W	R/W	R/W	R/W	
004H	TB3	D15	D14	D13	D12	0000
		R/W	R/W	R/W	R/W	
005H	DPL	A3	A2	A1	A0	0000
		R/W	R/W	R/W	R/W	
006H	DPM	A7	A6	A5	A4	0000
		R/W	R/W	R/W	R/W	
007H	DPH	A11	A10	A9	A8	0000
		R/W	R/W	R/W	R/W	
008H	PS	X	H/L	SLEEP	STOP	u100
		X	R/W	R/W	R/W	
009H	INTF	INT0F	TMR1F	INT1F	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	INT0IE	TMR1IE	INT1IE	TBIE	0000
		R/W	R/W	R/W	R/W	
00BH	Edge_LVR	RF1	RF0	LVREN	LVRC	0010
		R/W	R/W	R/W	R/W	
00CH	PAC	X	X	PAC1	PAC0	uu11
		X	X	R/W	R/W	
00DH	PA	X	PA2	PA1	PA0	u110
		X	R/W	R/W	R/W	
00EH	PBC	PBC3	PBC2	PBC1	PBC0	1111
		R/W	R/W	R/W	R/W	
00FH	PB	PB3	PB2	PB1	PB0	1111
		R/W	R/W	R/W	R/W	
010H	PCC	PCC3	PCC2	PCC1	PCC0	1111
		R/W	R/W	R/W	R/W	
011H	PC	PC3	PC2	PC1	PC0	1111
		R/W	R/W	R/W	R/W	
012H	PDC	X	PDC2	PDC1	PDC0	1111
		X	R/W	R/W	R/W	
013H	PD	X	PD2	PD1	PD0	1111
		X	R/W	R/W	R/W	

014H	PEC	PEC3	PEC2	PEC1	PEC0	1111
		R/W	R/W	R/W	R/W	
015H	PE	PE3	PE2	PE1	PE0	1111
		R/W	R/W	R/W	R/W	
016H	TBC/BZC	BZEN	TB2	TB1	TB0	0111
		R/W	R/W	R/W	R/W	
017H	TMR1L	TMR1_3	TMR1_2	TMR1_1	TMR1_0	0000
		R/W	R/W	R/W	R/W	
018H	TMR1H	TMR1_7	TMR1_6	TMR1_5	TMR1_4	0000
		R/W	R/W	R/W	R/W	
019H	TMR1C	TM1LD	T1CK1	T1CK0	TM1EN	0000
		R/W	R/W	R/W	R/W	
01AH	PWMADL	DTY13	DTY12	DTY11	DTY10	0000
		R/W	R/W	R/W	R/W	
01BH	PWMADH	DTY17	DTY16	DTY15	DTY14	0000
		R/W	R/W	R/W	R/W	
01CH	ADL	AD3	AD2	AD1	AD0	0000
		R	R	R	R	
01DH	ADH	AD7	AD6	AD5	AD4	0000
		R	R	R	R	
01EH	ADCTL0	ADEN	CH2	CH1	CH0	0000
		R/W	R/W	R/W	R/W	
01FH	ADCTL1	ADIE	ADF	ADCK1	ADCK0	0000
		R/W	R/W	R/W	R/W	
120H	PWMC	PWMBEN	PWMAEN	PWMBDC	PWMADC	0000
		R/W	R/W	R/W	R/W	
121H	AD-SEL0	AN3/PB3	AN2/PB2	AN1/PB1	AN0/PB0	0000
		R/W	R/W	R/W	R/W	
122H	AD-SEL1	AN7/PE3	AN6/PE2	AN5/PE1	AN4/PE0	0000
		R/W	R/W	R/W	R/W	
123H		X	X	X	X	uuuu
124H		X	X	X	X	uuuu
125H	PWMBDL	DTY23	DTY22	DTY21	DTY20	0000
		R/W	R/W	R/W	R/W	
126H	PWMBDH	DTY27	DTY26	DTY25	DTY24	0000
		R/W	R/W	R/W	R/W	
127H		X	X	X	X	uuuu
128H		X	X	X	X	uuuu

129H		X	X	X	X	uuuu
12AH	PWMCK	PWMBCK_S1	PWMBCK_S0	PWMACK_S1	PWMACK_S0	0000
		R/W	R/W	R/W	R/W	

3 : REGISTER Description

\$000(DP1) : Index == 虛擬指標暫存器

這不是一個實際的暫存器, 只用來當做間接定址的指標, 當對此位址讀寫或運算或讀取ROM TABLE 時, CPU 實際是以DPH, DPM, DPL 所組成的12 位元為地址線, 讀取ROM 的資料或是對RAM 做運算或讀寫資料。

\$001 : Acc == 累積器

除了當成一般暫存器使用外; 當需要將暫存器或RAM 的資料轉換到其他RAM 或暫存器時累積器是一個重要的中繼站, 先使用LDA 指令讀取暫存器或RAM 的資料暫存在累積器, 再用STX 指令存到想要存放的暫存器或RAM 中, 來達成暫存器或RAM 的資料轉換; 此外在做邏輯或算數運算時, 若是選擇結果放到Acc, 則運算完的結果將會存到累積器中; 在使用直接指令模式運算, 累積器是二個運算來源之一; 若是使用RTB 指令讀取ROM TABLE 時, 讀取到的資料是16 位元, 其中最低的4 位元(D3~D0) 也會暫存在累積器中

\$002 : TB1 == 讀表暫存器1

此暫存器提供我們在使用RTB 指令讀取ROM TABLE 時, 暫時存放讀取16 位元資料中的次低4 位元(D7~D4)用; 在不使用讀表功能時, 此暫存器可當作一般暫存器使用。

\$003 : TB2 == 讀表暫存器2

與TB1 同樣功能, 此暫存器提供我們在使用RTB 指令讀取ROM TABLE 時, 暫時存放讀取16 位元資料中的次高4 位元(D11~D8)用; 在不使用讀表功能時, 此暫存器可當作一般暫存器使用。

\$004 : TB3 == 讀表暫存器3

同樣的此暫存器提供我們在使用RTB 指令讀取ROM TABLE 時, 暫時存放讀取16 位元資料中的最高4 位元(D15~D12)用; 在不使用讀表功能時, 此暫存器可當作一般暫存器使用。

\$005 : DPL == 低位指標暫存器,

使用間接方式對RAM 位址讀寫或運算時, 此暫存器是指標(DP)的10 條地址線中最底的4 位元(A3~A0); 同時亦是使用RTB 指令讀取ROM TABLE 資料的12 位元地址線中最底的4 位元(A3~A0), 所以運用在上述二種方式使用之前必須先設定此暫存器。若是與上述的使用不衝突時可當作一般暫存器使用。

\$006 : DPM == 中位指標暫存器,

與DPL 功能相同, 在使用間接方式對RAM 位址讀寫或運算時, 此暫存器是指標(DP)

的10 條地址線之中間的4 位元(A7~A4);同時亦是使用RTB 指令讀取ROM TABLE 資料的12 位元地址線之中間的4 位元(A7~A4),所以運用在上述二種方式使用之前必須先設定此暫存器.若是與上述的使用不衝突時可當作一般暫存器使用.

\$007 : DPH == 高位指標暫存器,

與上述二暫存器功能相同,在使用間接方式對RAM 位址讀寫或運算時,此暫存器是指標(DP)的10 條地址線中最高的2 位元(A9~A8),A10 及A11 會被忽略掉一般設定為” 0”;同時亦是使用RTB 指令讀取ROM TABLE 資料的12 位元地址線中最高的4 位元(A11~A8),所以運用在上述二種方式使用之前必須先設定此暫存器.若是與上述的使用不衝突時可當作一般暫存器使用.

\$008 : PS == power saving register

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	X	H/L	SLEEP	STOP	1100
		X	R/W	R/W	R/W	

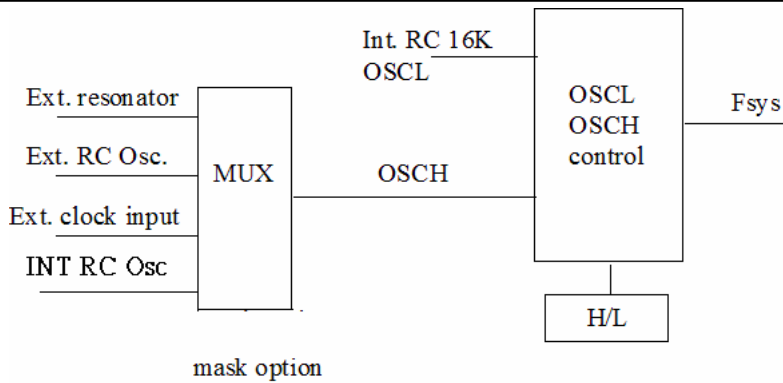
STOP(bit0) : high active ,=1 時 IC 進入 stop mode , All oscillator circuit is not active , cpu stop .

SLEEP(bit1) :high active ,=1 IC 進入 sleep mode , cpu stop , RC 16KHz oscillator On 。 高頻 oscillator 在 H/L (bit2)=1 時 on ; 在 H/L (bit2)=0 時 停振 .

Function status \ Operating mode	SLEEP(high active)	STOP(high active)
Oscillator	Operating	Stopped
CPU internal status	Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the executed address	
Timer/Counter/ Time base timer	Operated	Stopped & Retain
Watch-dog enable	Retain the status	
Release Condition(and clear STOP or SLEEP flag)	INT0/INT1/PA&PB & PC&PD &PE port Wake-up / ADC-INT(H/L=1)/ TMR1-INT(H/L=1)/ TB-INT	INT0/INT1/ PA&PB &PC&PD &PE port Wake-up/ TMR1_INT(select source = TMCK)

H/L(bit2) : Oscillator speed control register。

FLAG	FUNCTION
H/L	=0 : oscillator low speed mode (OSCL) =1 : oscillator high speed mode (OSCH)



* OSCL is always on except STOP=high.

* 如果進入 SLEEP MODE 時，若是 H/L 停在 low speed mode，此時 OSCH 要 off。

* 在 External RC oscillator mode 時，OSCO pin 會輸出 RC Osc. 頻率除以二的 clock 輸出。

* RTC oscillation stable time needs 0.5sec ~2 sec that depends on operating voltage and IC process.

interrupt control & request register

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	INT0F	TMR1F	INT1F	TBF	0000
		R/W0	R/W0	R/W0	R/W0	
00AH	INTC	INT0IE	TMR1IE	INT1IE	TBIE	0000
		R/W	R/W	R/W	R/W	

\$009H : interrupt request register

bit3 : INT0 (input pin PB0) interrupt request
bit1 : INT1 (input pin PB1) interrupt request
bit2 : timer1/counter1 interrupt request
bit0 : **Time Base Timer** interrupt request

INTF flag 會被 write bit “0” 時 clear 為 “0”，但是不會被 write bit “1” 時 set 為 “1”。

\$00AH : interrupt enable register

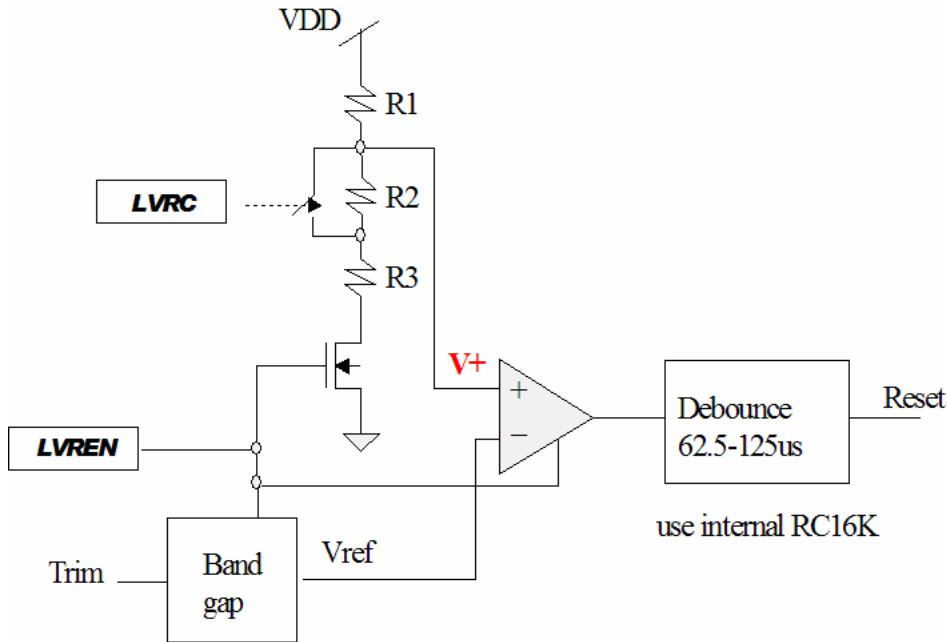
bit3 : INT0IE interrupt enable
bit1 : INT1IE interrupt enable
bit2 : timer1/counter1 interrupt enable
bit0 : **Time Base Timer** interrupt enable

Low Voltage Reset & INT0/INT1 edge trigger define

\$00BH :

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
00BH	Edge_LVR	RF1	RF0	LVREN	LVRC	0010
		R/W	R/W	R/W	R/W	

FLAG	FUNCTION
LVREN	Low : disable LVR function High : enable LVR function
LVRC	Low : select V+ level for LVR when LVREN=1 LVR 的偵測電壓為 $VDD < 2.2V \pm 10\%$ High : select V+ level for LVR when LVREN=1 LVR 的偵測電壓為 : $VDD < 3.0V \pm 10\%$



RF0/RF1：控制 interrupt INT0, INT1 的 trigger 方式。

RF1	RF0	Trigger
0	0	falling edge
0	1	rising edge
1	0	falling & rising edge
1	1	falling & rising edge

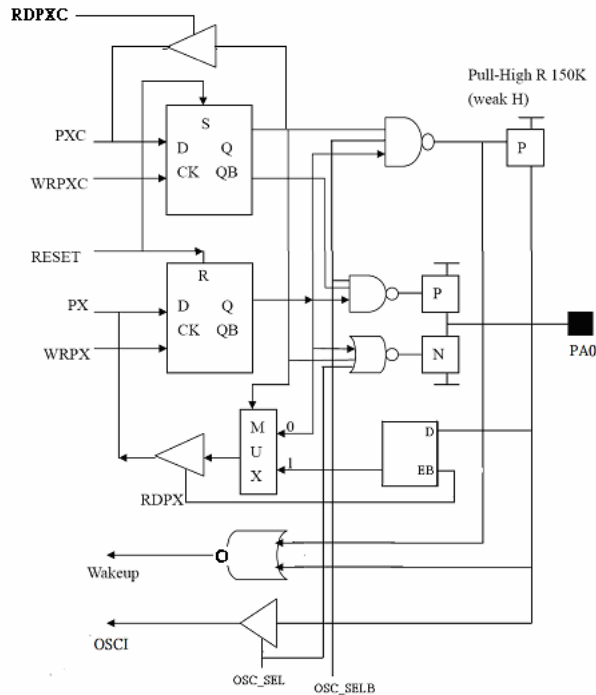
I/O REGISTER

Port A

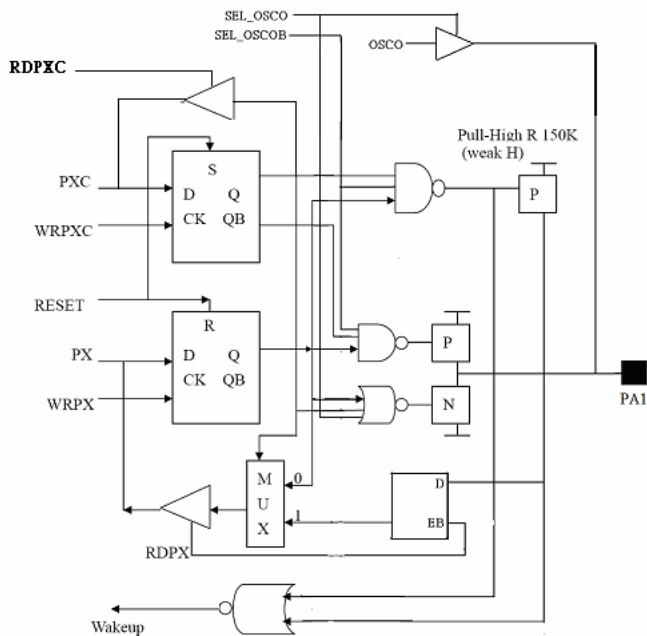
Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
00CH	PAC			PAC1	PAC0	uu11
				R/W	R/W	
00DH	PA		PA2	PA1	PA0	u110
			R/W	R/W	R/W	

PAC：是控制 I/O mode，為 high 時，是 input mode。

PA0：可 MASK option 為 osci 或為 I/O port，當選為 I/O port 時在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，(pull_high & PA0=0 時 wake_up=1) 如下圖。若選為 osci 時，PAC.bit0 PA.bit0 可當一般 memory 使用

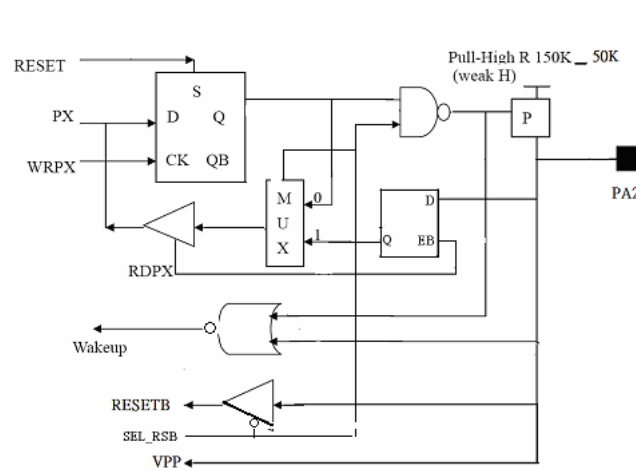


PA1：可 MASK option 為 osco 或為 I/O port，當選為 I/O port 時在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，(pull_high & PA1=0 時 wake_up=1) 如下圖。若選為 osci 時，PAC.bit1 PA.bit1 可當一般 memory 使用



PA2：可 MASK option 為 resetb 或為 input port，當選為 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，

(pull_high & PA2=0 時 wake_up=1) 如下圖。若選為 RESETB 時， PA.bit2 可當一般 memory 使用



Port B & Port E

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
00EH	PBC	PBC3	PBC2	PBC1	PBC0	1111
		R/W	R/W	R/W	R/W	
00FH	PB	PB3	PB2	PB1	PB0	1111
		R/W	R/W	R/W	R/W	
014H	PEC	PEC3	PEC2	PEC1	PEC0	1111
		R/W	R/W	R/W	R/W	
015H	PE	PE3	PE2	PE1	PE0	1111
		R/W	R/W	R/W	R/W	
01EH	ADCTL0	ADEN	CH2	CH1	CH0	0000
		R/W	R/W	R/W	R/W	
01FH	ADCTL1	ADIE	ADF	ADCK1	ADCK0	0000
		R/W	R/W	R/W	R/W	
121H	AD-SEL0	AN3/PB3	AN2/PB2	AN1/PB1	AN0/PB0	0000
		R/W	R/W	R/W	R/W	
122H	AD-SEL1	AN7/PE3	AN6/PE2	AN5/PE1	AN4/PE0	0000
		R/W	R/W	R/W	R/W	

PBC/ PEC：是控制 I/O mode，為 high 時，是 input mode。

PB/ PE：為 ADC channel 或 I/O port。由 AD-SEL1, AD-SEL0 register option，在 AD-SELx=0 時設為 I/O port data，

當設為 ADC channel 時 (AD-SELx=1) 相對的 PB, PBC bit 可當 memory 使用

當設定為 I/O port data 時

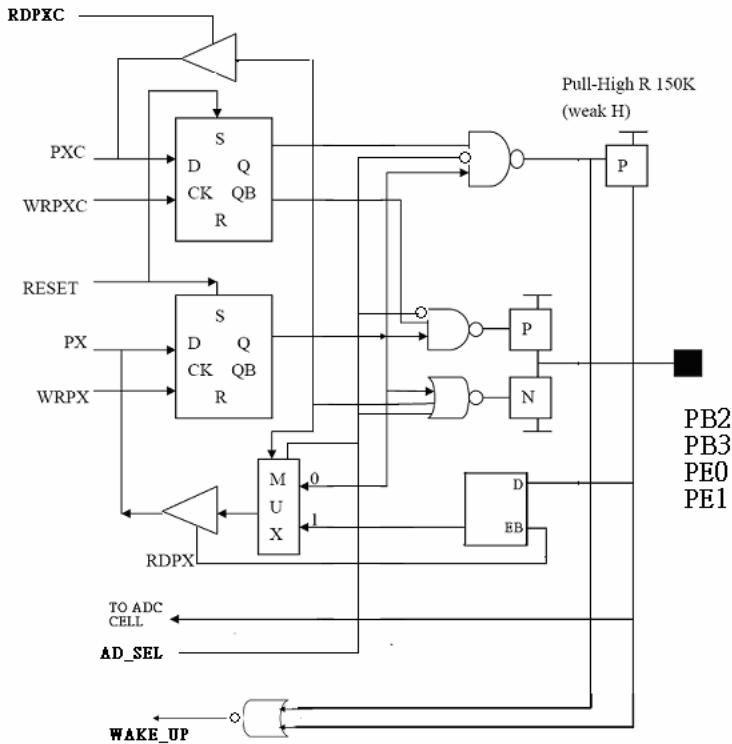
PB1/PB0 在 input mode 時 (Dreg) 可以控制是否有 pull high function。有 interrupt 功能 (rising and falling edge trigger 由 RF1, RF0 control)，當系統進入 STOP or SLEEP mode 時，可以用此 PIN 來 wake up。如下圖 Fig_PB0

PB3/PB2 在 input mode 時 (Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，(pull_high & input=0 使得 wake_up=1) 如下圖。
Fig_PB2

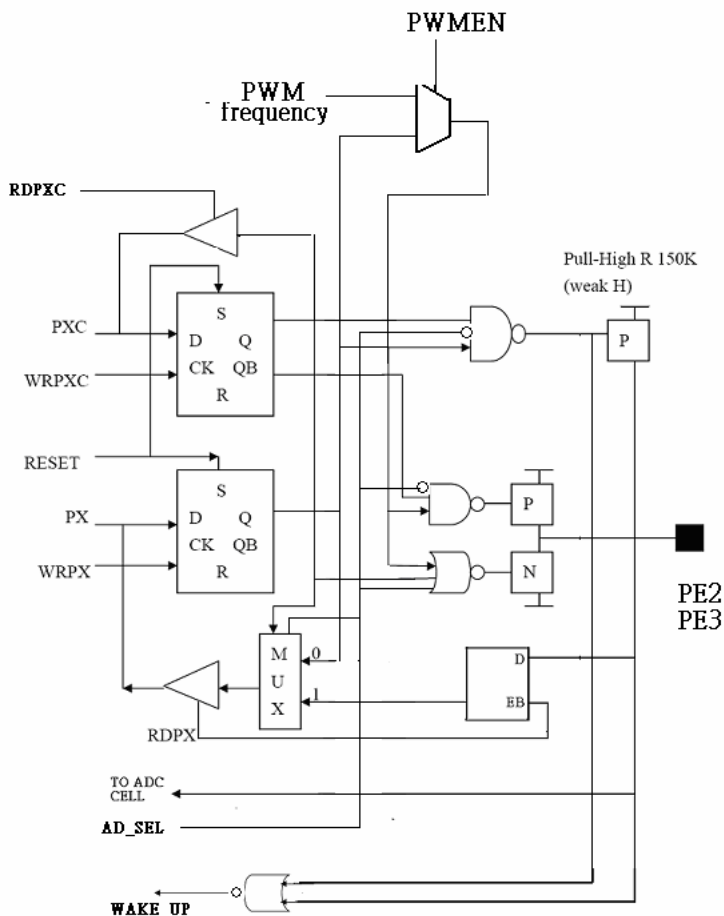
PE1/PE0 在 input mode 時 (Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，(pull_high & input=0 使得 wake_up=1) 如下圖。
Fig_PB2

PE3/PE2: 在 output mode (IOreg=0) & PWMxEN=1 時 為 PWM 輸出；
output mode (IOreg=0)& PWMxEN=0 時，輸出 PE3/PE2 data；
如果(IOreg=1)則為 input mode，在 input mode 時 (Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，(pull_high & input=0 使得 wake_up=1)如下圖。Fig_PE2





(Fig PB2)



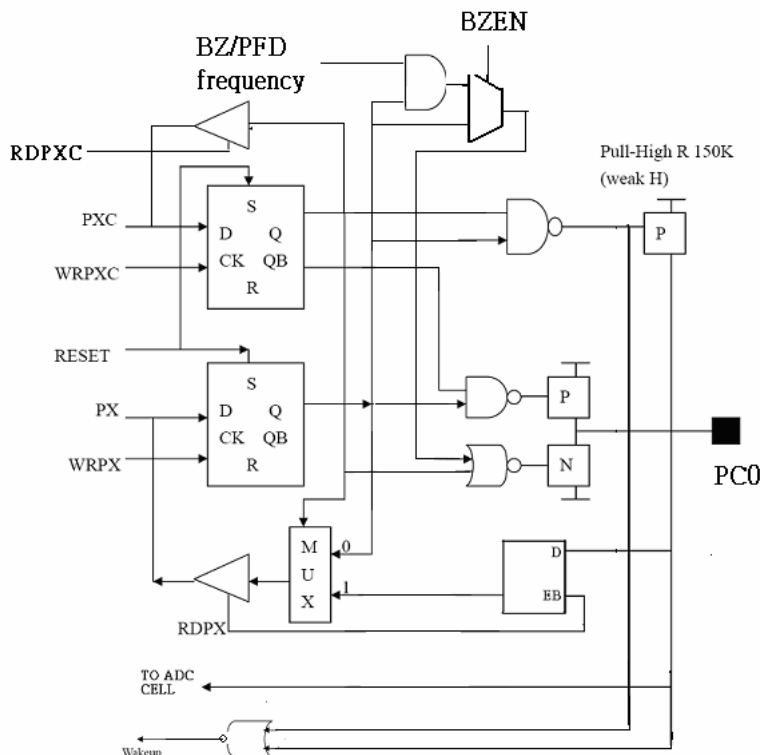
(Fig_PE2)

Port C & Port D

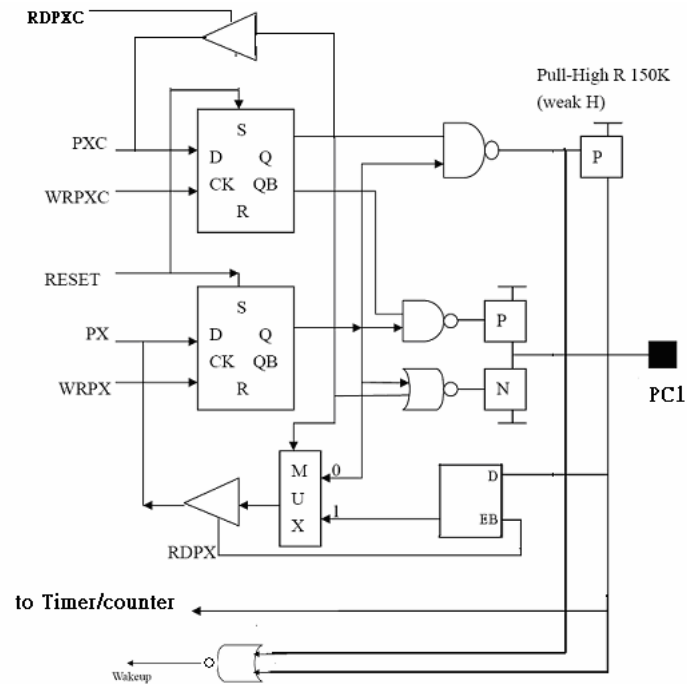
Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
010H	PCC	PCC3	PCC2	PCC1	PCC0	1111
		R/W	R/W	R/W	R/W	
011H	PC	PC3	PC2	PC1	PC0	1111
		R/W	R/W	R/W	R/W	
012H	PDC		PDC2	PDC1	PDC0	u111
			R/W	R/W	R/W	
013H	PD		PD2	PD1	PD0	u111
			R/W	R/W	R/W	

PCC/ PFC：是控制 I/O mode，為 high 時，是 input mode。

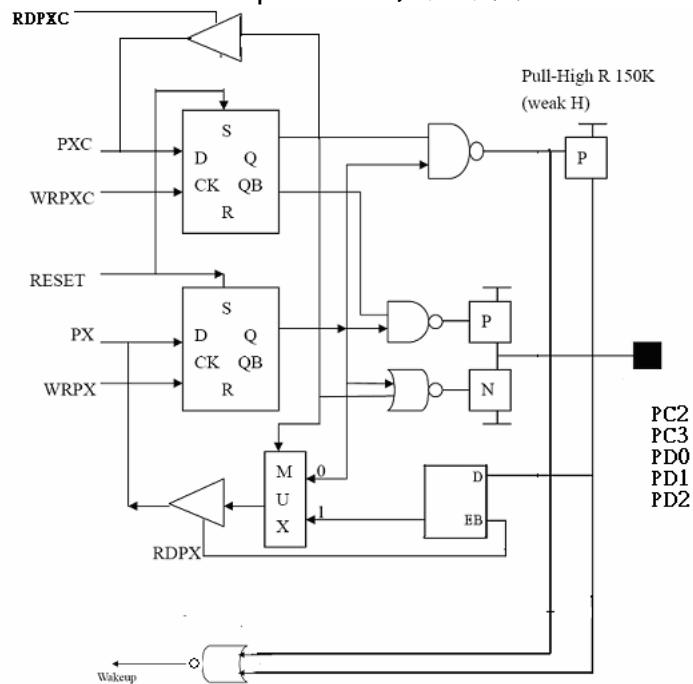
PC0：為 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function。在 output mode & BZEN=1 時，(Dreg) 可以控制是否有為 Buzzer/ PFD 輸出（當 Dreg=1 時輸出頻率，當 Dreg=0 時輸出為 low），如下圖。



PC1：為 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，如下圖。此 pin 亦可當作 Timer/Counter 的 clock input 如下圖。



PC2/PC3/PD0/PD1/PD2：為 I/O port data，在 input mode 時，（Dreg）可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，如下圖。



FLAG	FUNCTION
BZEN	LOW : PC0 without buzzer function HIGH : PC0 with buzzer function and enable buzzer frequency output through PC0 pad
PWMAEN	LOW : PE2 without PWM function, I/O function only HIGH : PE2 with PWM function or input function are controlled as below: - If (IOreg)=0 then enable PWMA frequency output through pad - If (IOreg)=1 then at input function mode
PWMBEN	LOW : PE3 without PWM function, I/O function only HIGH : PE3 with PWM function or input function are controlled as below: - If (IOreg)=0 then enable PWMB frequency output through pad - If (IOreg)=1 then at input function mode

1 Time Base Timer

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
016H	TBC/BZC	BZEN	TB2	TB1	TB0	0111
		R/W	R/W	R/W	R/W	

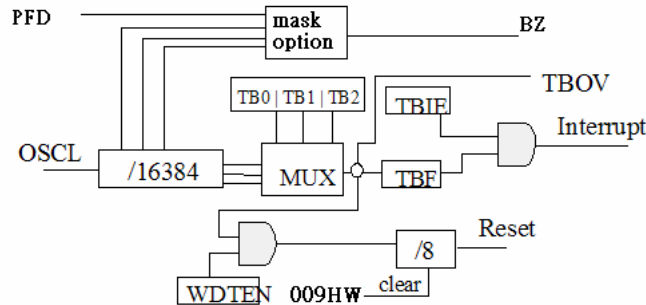
TBF : Time base timer overflow flag。 (此 flag 會被 write bit “0” 時 clear 為 “0”，但是不會被 write bit “1” 時 set 為 “1”)

TBIE : Time base timer interrupt enable control register。

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	INT0F	TMR1F	INT1F	TBF	0000
		R/W0	R/W0	R/W0	R/W0	
00AH	INTC	INT0IE	TMR1IE	INT1IE	TBIE	0000
		R/W	R/W	R/W	R/W	

TB0/ TB1/ TB2 : Time base timer input clock source select register。

TB2	TB1	TB0	O/P
0	0	0	128HZ
0	0	1	64HZ
0	1	0	32HZ
0	1	1	16HZ
1	0	0	8HZ
1	0	1	4HZ
1	1	0	2HZ
1	1	1	1HZ



2 Watch Dog Timer :

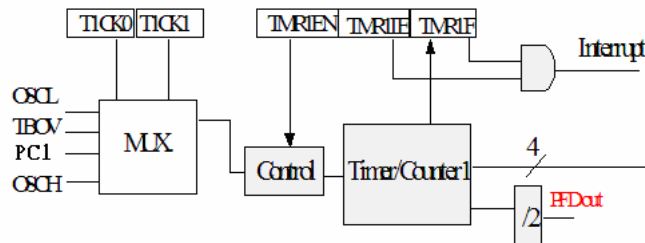
Watch Dog overflow 的時間 為 TBOV 的 7~8 倍 (clear WDT 無法清除 Time base 所以 為 TBOV 的 7~8 倍) , (power on default 為 7~8 秒)
clear WDT 的方法 為 wirite \$F to INTF flag 來clear WDT，如上圖。

3 8-bit Timer1/Counter1 function description

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
017H	TMR1L	TMR1_3	TMR1_2	TMR1_1	TMR1_0	0000
		R/W	R/W	R/W	R/W	
018H	TMR1H	TMR1_7	TMR1_6	TMR1_5	TMR1_4	0000
		R/W	R/W	R/W	R/W	
019H	TMR1C	TM1LD	T1CK1	T1CK0	TM1EN	0000
		R/W	R/W	R/W	R/W	

TMR1L/ TMR1H/ : Timer/Counter data, Timer/Counter 的 data 可以 R/W。Overflow 時會 set interrupt flag (TMR1F/)

FLAG	FUNCTION
TM1EN	Low : stop Timer/Counter1 High : start Timer/Counter1
TM1LD	Low : without Auto-reload function(Timer/Counter1) High : with Auto-reload function(Timer/Counter1)
T1CK1/ T1CK0	(T1CK1/ T1CK0) 00 : select OSCH clock 01 : select time base timer clock(OSCL) 10 : select PC1 external input clock 11 : select time base timer overflow(TBOV)



4 PWM CONTROL CIRCUIT

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
01AH	PWMADL	DTY13	DTY12	DTY11	DTY10	0000
		R/W	R/W	R/W	R/W	
01BH	PWMADH	DTY17	DTY16	DTY15	DTY14	0000
		R/W	R/W	R/W	R/W	
120H	PWMC	PWMBEN	PWMAEN	PWMBDC	PWMADC	0000
		R/W	R/W	R/W	R/W	
125H	PWMBDL	DTY23	DTY22	DTY21	DTY20	0000
		R/W	R/W	R/W	R/W	
126H	PWMBDH	DTY27	DTY26	DTY25	DTY24	0000
		R/W	R/W	R/W	R/W	
12AH	PWMCK	PWMBCK_ S1	PWMBCK_ S0	PWMACK_ S1	PWMACK_ S0	0000
		R/W	R/W	R/W	R/W	

PWMADL, PWMADH, PWMBDL, PWMBDH: 控制 PWM 的 duty. (register option 2 modes)

FLAG	FUNCTION
PWMAEN	Low : disable PWMA output High : enable PWMA output
PWMBEN	Low : disable PWMB output High : enable PWMB output
PWMADC	Low : PWM circuit in 4 duty mode when PWMAEN is high state High : PWM circuit in 2 duty mode when PWMAEN is high state
PWMBDC	Low : PWM circuit in 4 duty mode when PWMBEN is high state High : PWM circuit in 2 duty mode when PWMBEN is high state
PWMACK_S1/ PWMACK_S0	Select PWMA input clock 00 : high frequency, 01: high frequency/4 10 : high frequency/16, 11: high frequency/64
PWMBCK_S1/ PWMBCK_S0	Select PWMB input clock 00 : high frequency, 01: high frequency/4 10 : high frequency/16, 11: high frequency/64

4 duty cycle mode :

DTY*7	DTY*6	DTY*5	DTY*4	DTY*3	DTY*2	DTY*1	DTY*0	4 Duty Cycles
0	0	0	0	0	0	0	0	0/64+0/64+0/64+0/64
0	0	0	0	0	0	0	1	1/64+0/64+0/64+0/64
0	0	0	0	0	0	1	0	1/64+1/64+0/64+0/64
0	0	0	0	0	0	1	1	1/64+1/64+1/64+0/64
0	0	0	0	0	1	0	0	1/64+1/64+1/64+1/64
...	...	...	...	...	...	...	...	...
0	1	0	0	0	0	0	1	17/64+16/64+16/64+16/64
0	1	0	0	0	0	1	0	17/64+17/64+16/64+16/64

0	1	0	0	0	0	1	1	17/64+17/64+17/64+16/64
0	1	0	0	0	1	0	0	17/64+17/64+17/64+17/64
...	...	...	...	...	...	...	...	...
1	0	0	0	0	0	0	1	33/64+32/64+32/64+32/64
1	0	0	0	0	0	1	0	33/64+33/64+32/64+32/64
1	0	0	0	0	0	1	1	33/64+33/64+33/64+32/64
1	0	0	0	0	1	0	0	33/64+33/64+33/64+33/64
...	...	...	...	...	...	...	...	...
1	1	0	0	0	0	0	1	49/64+48/64+48/64+48/64
1	1	0	0	0	0	1	0	49/64+49/64+48/64+48/64
1	1	0	0	0	0	1	1	49/64+49/64+49/64+48/64
1	1	0	0	0	1	0	0	49/64+49/64+49/64+49/64
...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	0	0	63/64+63/64+63/64+63/64
1	1	1	1	1	1	0	1	64/64+63/64+63/64+63/64
1	1	1	1	1	1	1	0	64/64+64/64+63/64+63/64
1	1	1	1	1	1	1	1	64/64+64/64+64/64+63/64

2 duty cycle mode :

DTY*7	DTY*6	DTY*5	DTY*4	DTY*3	DTY*2	DTY*1	DTY*0	2 Duty Cycles
0	0	0	0	0	0	0	0	0/128+0/128
0	0	0	0	0	0	0	1	1/128+0/128
0	0	0	0	0	0	1	0	1/128+1/128
0	0	0	0	0	0	1	1	2/128+1/128
0	0	0	0	0	1	0	0	2/128+2/128
...	...	...	...	...	...	...	...	...
0	1	0	0	0	0	0	1	33/128+32/128
0	1	0	0	0	0	1	0	33/128+33/128
0	1	0	0	0	0	1	1	34/128+33/128
0	1	0	0	0	1	0	0	34/128+34/128
...	...	...	...	...	...	...	...	...
1	0	0	0	0	0	0	1	65/128+64/128
1	0	0	0	0	0	1	0	65/128+65/128
1	0	0	0	0	0	1	1	66/128+65/128
1	0	0	0	0	1	0	0	66/128+66/128
...	...	...	...	...	...	...	...	...
1	1	0	0	0	0	0	1	97/128+96/128
1	1	0	0	0	0	1	0	97/128+97/128
1	1	0	0	0	0	1	1	98/128+97/128
1	1	0	0	0	1	0	0	98/128+98/128
...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	0	0	126/128+126/128
1	1	1	1	1	1	0	1	127/128+126/128
1	1	1	1	1	1	1	0	127/128+127/128
1	1	1	1	1	1	1	1	128/128+127/128

5 A/D function description

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
01CH	ADL	AD3	AD2	AD1	AD0	0000
		R	R	R	R	
01DH	ADH	AD7	AD6	AD5	AD4	0000
		R	R	R	R	
01EH	ADCTL0	ADEN	CH2	CH1	CH0	0000
		R/W	R/W	R/W	R/W	
01FH	ADCTL1	ADIE	ADF	ADCK1	ADCK0	0000
		R/W	R/W	R/W	R/W	
121H	AD-SEL0	AN3/PB3	AN2/PB2	AN1/PB1	AN0/PB0	0000
		R/W	R/W	R/W	R/W	
122H	AD-SEL1	AN7/PE3	AN6/PE2	AN5/PE1	AN4/PE0	0000
		R/W	R/W	R/W	R/W	

\$121H & 122H : 選擇 PAD 是 I/O port (data=0) 或 AD port (data=1)

\$01CH & 01DH ADL/ADH : (AD0-AD7) 是 A/D 的 DATA。

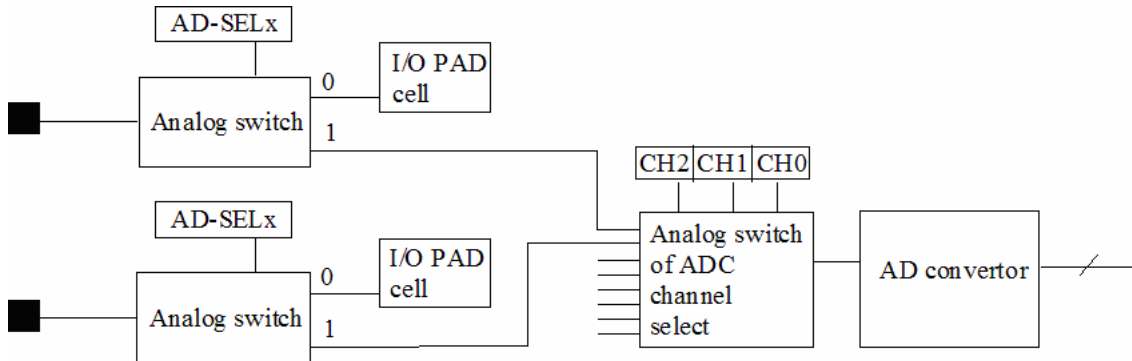
如果對此 01CH PORT 做 WRITE 的動作時, 要讓 ADC START CONVERSION。

如果對此 01DH PORT 做 WRITE 的動作時, 要讓 CPU SLEEP & ADC START CONVERSION。

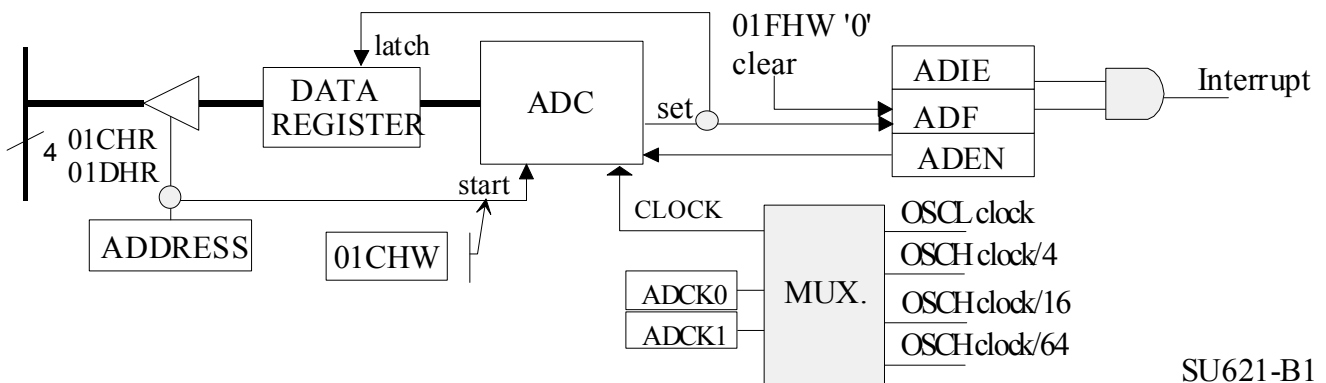
\$01EH & 01FH : ADCTL0/ ADCTL1 : 是 A/D 的 CONTROL REGISTER。

FLAG	FUNCTION
ADIE	LOW : Disable internal interrupt HIGH : Enable internal interrupt
ADF	LOW : Normal mode HIGH : A/D conversion complete flag。此 flag 會被 write bit “0” 時 clear 為 “0”, 但是不會被 write bit “1” 時 set 為 “1”
ADEN	LOW : Disable A/D HIGH : Enable A/D
CH2 CH1 CH0	(CH2/CH1/CH0) 000 : select AN0 input, 001 : select AN1 input, 010 : select AN2 input, 011 : select AN3 input, 100 : select AN4 input, 101 : select AN5 input, 110 : select AN6 input, 111 : select AN7 input。
ADCK1 ADCK0	(ADCK1/ ADCK0)

	00 : select OSCL clock, 01 : select OSCH clock/4, 10 : select OSCH clock/16, 11 : select OSCH clock/64.
--	--



CH2	CH1	CH0	ADC channel selection
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7



SU621-B1

當 ADC 完成 conversion 後，才 latch “ADL” 和 “ADH” 的 data。

Instruction set :

ins	expression	operation	types	word/cycles	store	psw
ADC	ADC #x,\$xx,A	M+op+c ---> A	IO R&W	1/1	A	z,c
ADC	ADC #x,\$xx,M	M+op+c ---> M	IO R&W	1/1	M	z,c
ADC	ADC \$xxx,A	M+A+c ---> A	IO R&W	1/1	A	z,c
ADC	ADC \$xxx,M	M+A+c ---> M	IO R&W	1/1	M	z,c
ADD	ADD #x,\$xx,A	M+op ---> A	IO R&W	1/1	A	z,c
ADD	ADD #x,\$xx,M	M+op ---> M	IO R&W	1/1	M	z,c
ADD	ADD \$xxx,A	M+A ---> A	IO R&W	1/1	A	z,c
ADD	ADD \$xxx,M	M+A ---> M	IO R&W	1/1	M	z,c
SBC	SBC #x,\$xx,A	M-op-c ---> A	IO R&W	1/1	A	z,c
SBC	SBC #x,\$xx,M	M-op-c ---> M	IO R&W	1/1	M	z,c
SBC	SBC \$xxx,A	M-A-c ---> A	IO R&W	1/1	A	z,c
SBC	SBC \$xxx,M	M-A-c ---> M	IO R&W	1/1	M	z,c
SUB	SUB #x,\$xx,A	M-op ---> A	IO R&W	1/1	A	z,c
SUB	SUB #x,\$xx,M	M-op ---> M	IO R&W	1/1	M	z,c
SUB	SUB \$xxx,A	M-A ---> A	IO R&W	1/1	A	z,c
SUB	SUB \$xxx,M	M-A ---> M	IO R&W	1/1	M	z,c
ORI	ORI #x,\$xx,A	M op ---> A	IO R&W	1/1	A	z
ORI	ORI #x,\$xx,M	M op ---> M	IO R&W	1/1	M	z
ORI	ORI \$xxx,A	M A ---> A	IO R&W	1/1	A	z
ORI	ORI \$xxx,M	M A ---> M	IO R&W	1/1	M	z
XOR	XOR #x,\$xx,A	M ^ op ---> A	IO R&W	1/1	A	z
XOR	XOR #x,\$xx,M	M ^ op ---> M	IO R&W	1/1	M	z
XOR	XOR \$xxx,A	M ^ A ---> A	IO R&W	1/1	A	z
XOR	XOR \$xxx,M	M ^ A ---> M	IO R&W	1/1	M	z
AND	AND #x,\$xx,A	M & op ---> A	IO R&W	1/1	A	z
AND	AND #x,\$xx,M	M & op ---> M	IO R&W	1/1	M	z
AND	AND \$xxx,A	M & A ---> A	IO R&W	1/1	A	z
AND	AND \$xxx,M	M & A ---> M	IO R&W	1/1	M	z
CMP	CMP #x,\$xx	M - op	IO R	1/1		z,c
CMP	CMP \$xxx	M - A	IO R	1/1		z,c
TST	TST #x,\$xx	M & op	IO R	1/1		z
TST	TST \$xxx	M & A	IO R	1/1		z
RTS	RTS	return CAL	return	1/1		pc
LDA	LDA \$xxx	M ---> A	IO R	1/1	A	z

STX	STX #x,\$xx	op ---> M	IO W	1/1	A/M	
STX	STX \$xxx	A ---> M	IO W	1/1	A/M	
RLC	RLC \$xxx,A	c <-- M <-- c --->A	IO RW	1/1	A	z,c
RLC	RLC \$xxx,M	c <-- M <-- c --->M	IO RW	1/1	M	z,c
RRC	RRC \$xxx,A	c --> M --> c --->A	IO RW	1/1	A	z,c
RRC	RRC \$xxx,M	c --> M --> c --->M	IO RW	1/1	M	z,c

ins	expression	operation	types	word/cycles	store	psw
LDP	LDP \$xxx	op ---> DP1H,DP1M,DP1L	DP W	1/1	DP1	DP1
RTB	RTB \$xxx	op ---> tb3,tb2,tb1,A	ROM R	1/2		
RTI	RTI	return INT	return	1/1		pc,z,c
JMP	JMP \$xxx	op ---> PC	force Jump	1/1	PC	pc
CDP	CDP	clear DP1 auto INC	control DP1	1/1		e=0
JPC	JPC \$xxx	If c=1 then op ---> PC	condition Jump	1/1	PC	pc
SDP	SDP	set DP1 auto INC	control DP1	1/1		e=1
JPZ	JPZ \$xxx	If z=1 then op ---> PC	condition Jump	1/1	PC	pc
SEC	SEC	set flag c=1	set c flag	1/1		c=1
CAL	CAL \$xxx	Call subroutine op ---> PC	Jump sub.	1/1	PC	pc
CLC	CLC	clear flag c=1	clear c flag	1/1		c=0

RESET PLAN

Reset 方式有 3 種：

A. Power on RESET

B. EXTERNAL RESET (ACTIVE LOW)

C. LVR RESET (單邊 reset, high voltage to low voltage)

.Mask option table

Function	Option
Oscillator type	☐ Resonator。 ☐ external RC oscillator。 ☐ internal RC oscillator。
RESERTB	☐ Resetb port ☐ PA2 port
LVR control	☐ LVR disable ☐ LVR enable
Buzzer frequency selection	☐ 2KHZ。 ☐ 4KHZ。 ☐ 6KHZ。 ☐ PFD。

Low voltage detect , system reset 時 IC 會自動將 mask_option 內的 data load 到 00BH.bit1, 當初始值.

. External RC oscillator Resistor vs. Frequency table

電阻 (Ω)	電壓(V)	頻率(Hz)
51K	5	7.3M
56K	5	6.6M
62K	5	6.1M
68K	5	5.4M
75K	5	4.7M
82K	5	4.4M
91K	5	4.1M
100K	5	3.7M
120K	5	3.1M
150K	5	2.4M
160K	5	2.3M
180K	5	2.0M
200K	5	1.8M
220K	5	1.7M
240K	5	1.6M
300K	5	1.2M



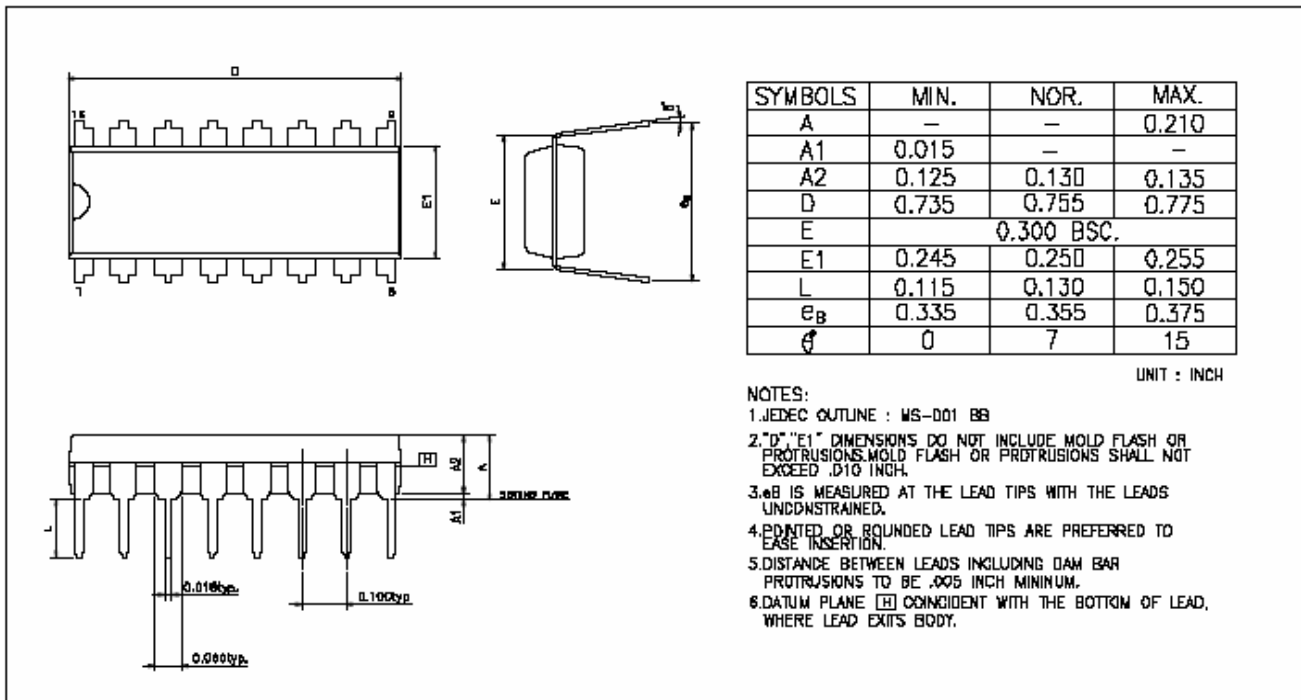
510K	5	714K
1M	5	368K

. ORDER INFORMATION

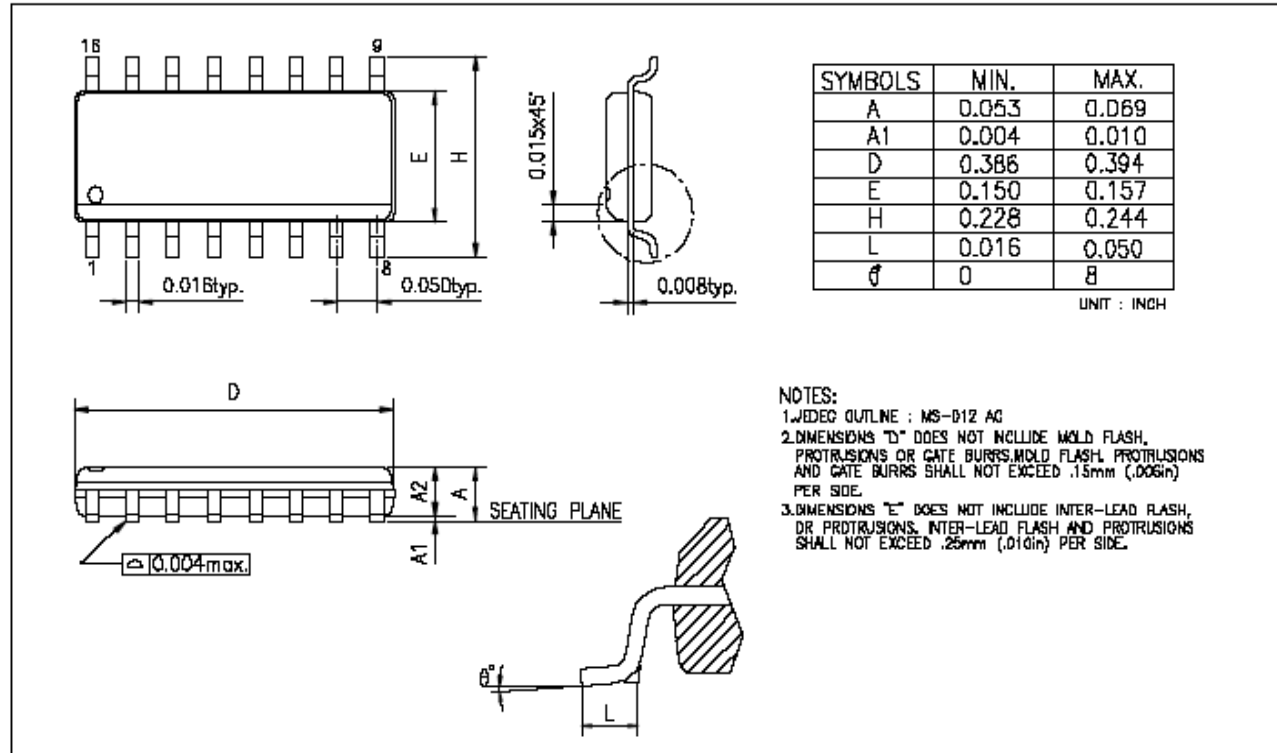
- a. Package form : TTR620
- b. Chip form : TCR620
- c. Wafer base : TDR620

Package Information

(16-DIP)

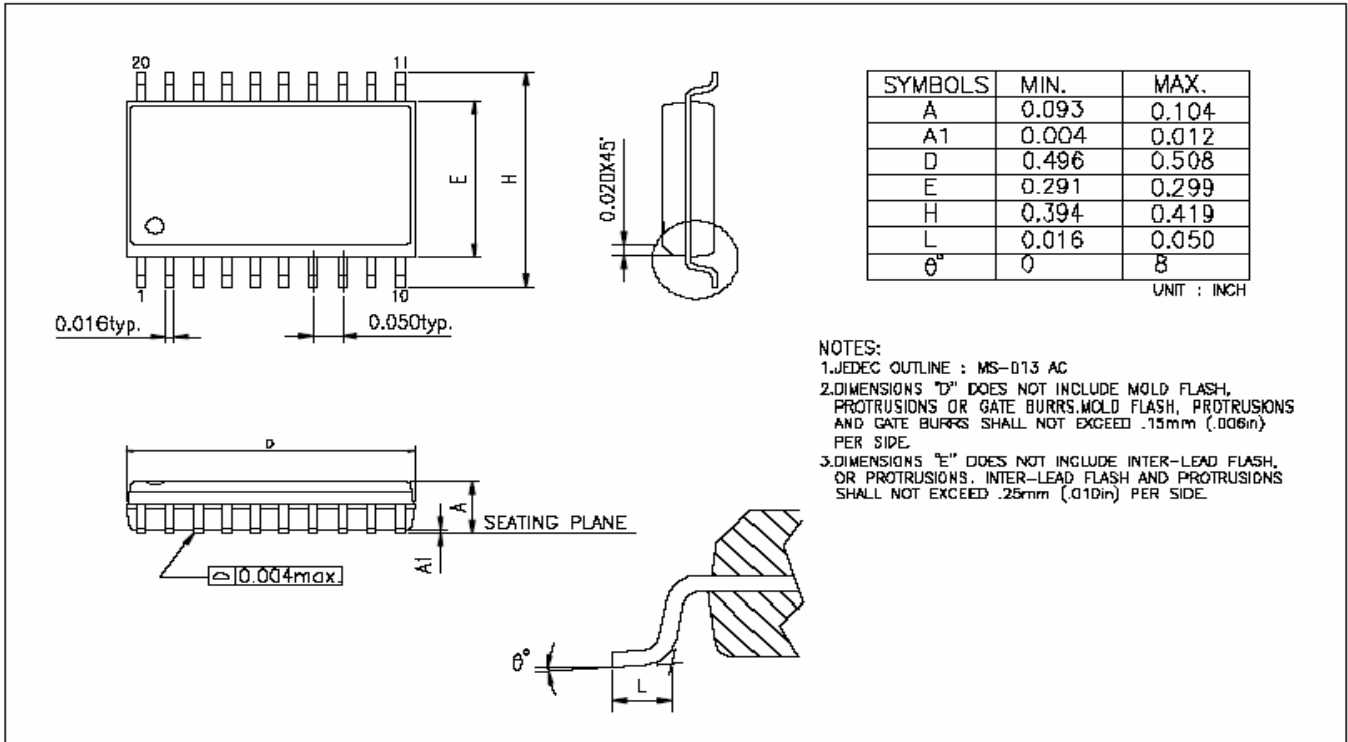


(16-SOP)



(20-SKINNY DIP)

(20-SOP)





Revise History

Date	Name	Version	Page	Content
2009/7/1	Eric_ch	V3.0-000	1-37	Preliminary