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1. FEATURES

• **CPU**

8 Bit CISC Core(8051 Compatible)

• **ROM (FLASH) capacity**

12K Bytes
Flash with self read/write capability
On chip debug and In-system programming (ISP)
Endurance: 10,000 times (Sector 0~379)
100,000 times (Sector 380~383)
Retention: 10 Years (Min)

• **SRAM capacity**

256 Bytes (Excluding 32 Bytes for LCD Display)

• **General Purpose I/O (GPIO)**

6 I/O, 39 Shared I/O with LCD signal

• **Basic Interval Timer (BIT)**

8Bit × 1ch

• **Watch Dog Timer (WDT)**

8Bit × 1ch, 5kHz internal RC oscillator

• **Timer/ Counters**

8Bit x 2ch (T0/T1), 16Bit x 2ch (T2/T3)
16Bit Interval Timer × 1ch

• **Carrier Generation**

Carrier generation (by T1), T3 Clock source

• **Programmable Pulse Generation**

Pulse generation by T2/T3

• **Watch Timer (WT)**

3.91ms/0.25s/0.5s/1s/1M interval at 32.768kHz

• **Built-in Transistor for I.R LED Drive**

IOL = 630mA at 3V and VOL = 1.0V

• **Built-in Transistor for LCD Back Light Drive**

2Pins, IOL = 10/20/30 [mA] at 3V and VOL = 1.0V

• **LCD Driver**

26 Segments and 8 Common
1/2, 1/3, 1/4, 1/5, 1/6, 1/8 duty selectable
Voltage booster and 16-step contrast control
Internal/External resistor bias

• **10 Bit A/D Converter**

8 Input channels

• **16-Bit CRC/Checksum Generator**

Auto and User CRC/Checksum mode

• **Inverter Amplifier**

3-ch high-gain inverter amplifiers

• **Power On Reset**

Reset release level (1.2V)

• **Low Voltage Reset**

4 Level detect (1.62V, 2.0V, 2.4V, 2.68V)

• **Low Voltage Indicator**

3 Level detect (2.0V, 2.4V, 2.68V)

• **Interrupt Source**

External interrupts (EINT0,,,EINT7,EINT12/13)
Timer 0,,,,,3, WDT, BIT, WT, LVI

• **Internal RC Oscillator**

HFIRC: 8MHz ± 1.0%(T_A=-10 ~ +55°C, User trim)
LFIRC: 32kHz ± 10.0%(T_A = -10 ~ +55°C)

• **Power Down Mode**

Stop and Idle mode

• **Operating Voltage & Frequency**

1.8V to 3.6V @ 32 to 38kHz with SX-tal
1.8V to 3.6V @ 0.4 to 4.2MHz with X-tal, Ceramic
2.0V to 3.6V @ 0.4 to 4.2MHz with X-tal, Crystal
2.4V to 3.6V @ 0.4 to 8.0MHz with X-tal
3.0V to 3.6V @ 0.4 to 12.0MHz with X-tal
1.8V to 3.6V @ 0.5 to 8.0MHz with HFIRC
1.8V to 3.6V @ 4.0 to 32.0kHz with LFIRC
Voltage dropout converter included for core

• **Minimum Instruction Execution Time**

167ns at 12MHz main clock
61us at 32.768kHz sub clock

• **Operating Temperature**

–40 to +85℃

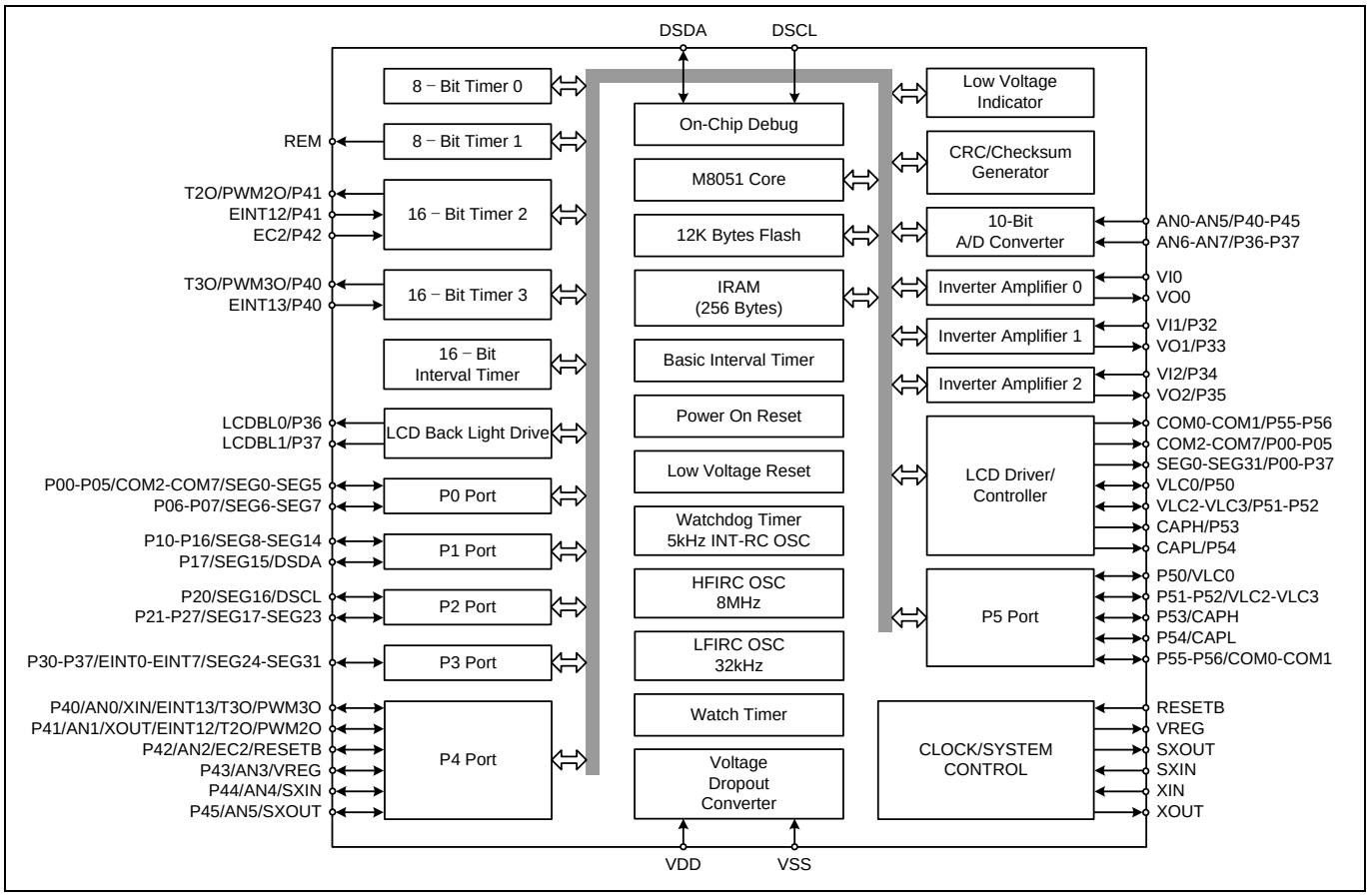
• **Oscillator Type**

0.4-12MHz crystal or ceramic for main clock
32.768kHz crystal for sub clock

• **Package**

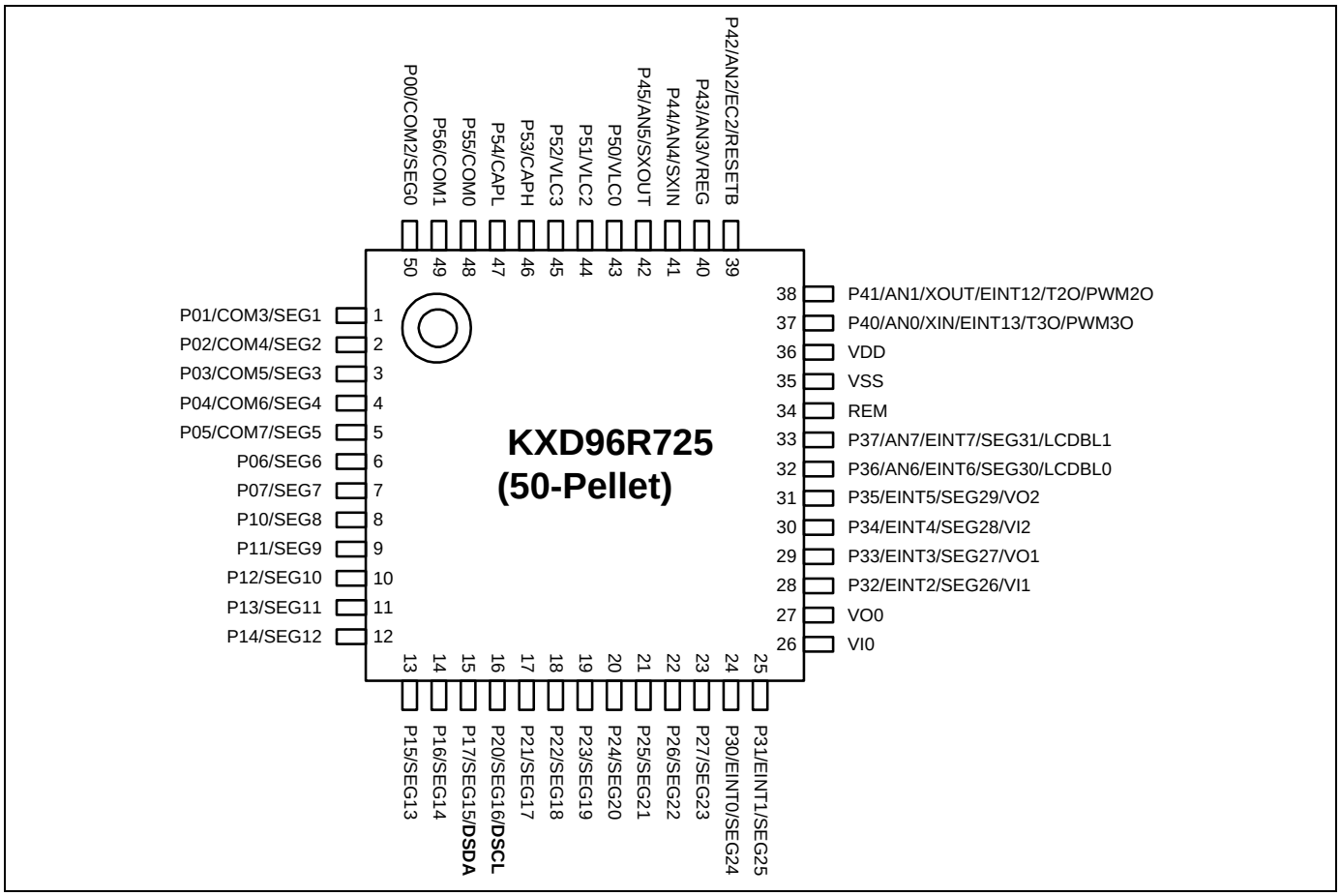
50-Pin Pellet, 48 LQFP-0707, Pb-free package

2. BLOCK DIAGRAM

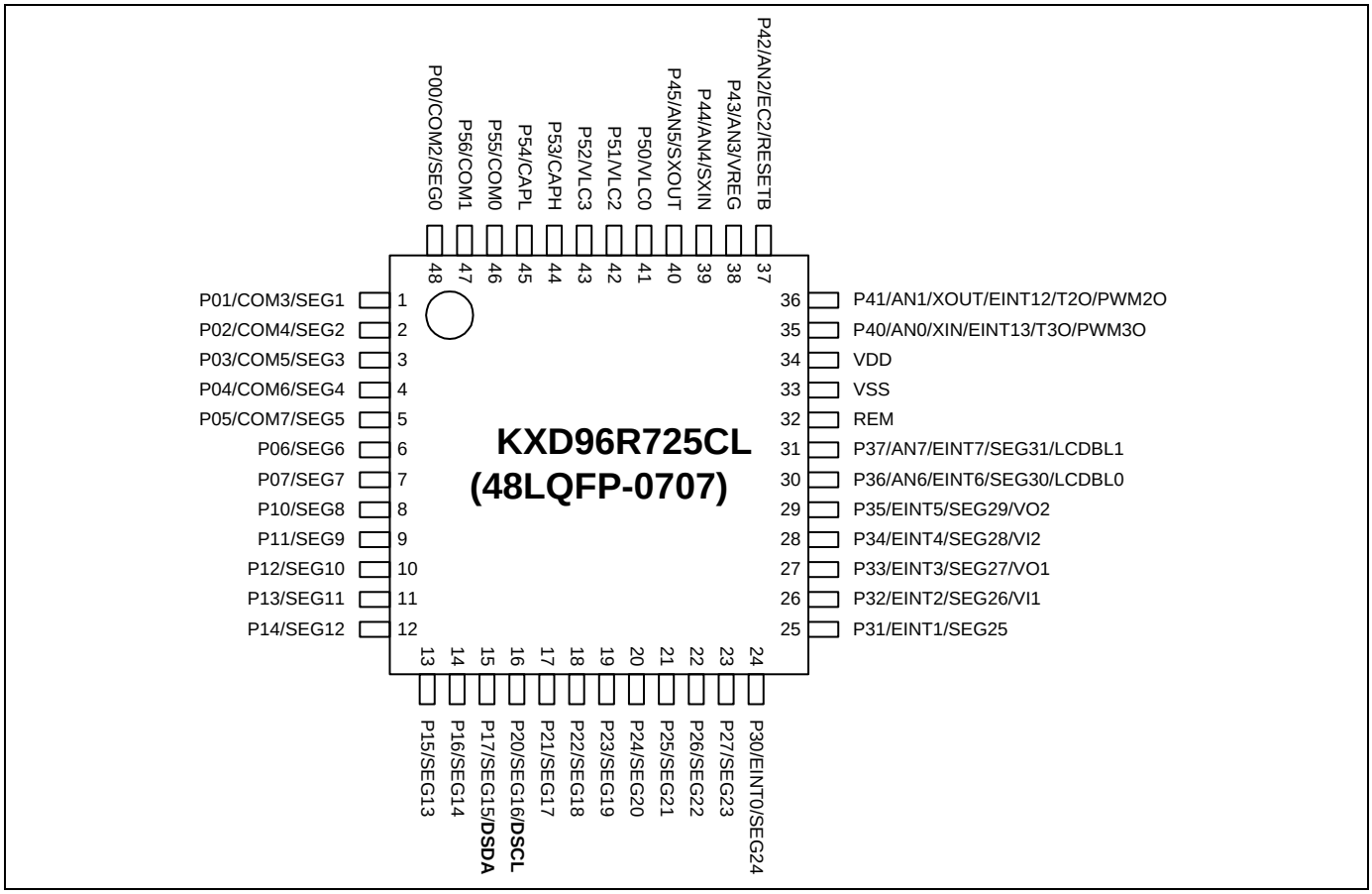


3. PIN ASSIGNMENTS

3.1 50 PIN-PELLET



3.1 48 PIN-LQFP



4. PIN DESCRIPTIONS

Pin Names	I/O	Pin Description	After RESET	Alternative Functions
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	COM2/SEG0
P01				COM3/SEG1
P02				COM4/SEG2
P03				COM5/SEG3
P04				COM6/SEG4
P05				COM7/SEG5
P06				SEG6
P07				SEG7
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as an input (P17: Schmitt-trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG8
P11				SEG9
P12				SEG10
P13				SEG11
P14				SEG12
P15				SEG13
P16				SEG14
P17				SEG15/DSDA
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input (P20: Schmitt-trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG16/DSCL
P21				SEG17
P22				SEG18
P23				SEG19
P24				SEG20
P25				SEG21
P26				SEG22
P27				SEG23
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT0/SEG24
P31				EINT1/SEG25
P32				EINT2/SEG26/VI1
P33				EINT3/SEG27/VO1
P34				ENIT4/SEG28/VI2
P35				EINT5/SEG29/VO2
P36				AN6/EINT6/SEG30/LCDBL0
P37				AN7/EINT7/SEG31/LCDBL1

Pin Names	I/O	Pin Description	After RESET	Alternative Functions
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0/XIN/EINT13/T3O/PWM3O
P41				AN1/XOUT/EINT12/T2O/PWM2O
P42				AN2/EC2/RESETB
P43				AN3/VREG
P44				AN4/SXIN
P45				AN5/SXOUT
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	VLC0
P51				VLC2
P52				VLC3
P53				CAPH
P54				CAPL
P55				COM0
P56				COM1
EINT0	I/O	External interrupt inputs	Input	P30/SEG24
EINT1				P31/SEG25
EINT2				P32/SEG26
EINT3				P33/SEG27
EINT4				P34/SEG28
EINT5				P35/SEG29
EINT6				P36/SEG30
EINT7				P37/SEG31
EINT12	I/O	External interrupt and Timer 12 capture input	Input	P41/AN1/XOUT/T2O/PWM2O
EINT13	I/O	External interrupt and Timer 13 capture input	Input	P40/AN0/XIN/T3O/PWM3O
T2O	I/O	Timer 12 interval output	Input	P41/AN1/XOUT/EINT12/PWM2O
T3O	I/O	Timer 13 interval output	Input	P40/AN0/XIN/EINT13/PWM3O
PWM2O	I/O	Timer 12 pulse output	Input	P41/AN1/XOUT/EINT12/T2O
PWM3O	I/O	Timer 13 pulse output	Input	P40/AN0/XIN/EINT13/T3O
EC2	I/O	Timer 13 event count input	Input	P42/AN2/RESETB
AN0	I/O	A/D converter analog input channels	Input	P40/XIN/EINT13/T3O/PWM3O
AN1				P41/XOUT/EINT12/T2O/PWM2O
AN2				P42/EC2/RESETB
AN3				P43/VREG
AN4				P44/SXIN
AN5				P45/SXOUT
AN6				P36/EINT6/SEG30/LCDBL0
AN7				P37/EINT7/SEG31/LCDBL1

Pin Names	I/O	Pin Description	After RESET	Alternative Functions
REM	O	High current n-channel open-drain output for driving I.R. LED.	Output	–
LCDBL0	I/O	LCD back light drive pins	Input	P36/AN6/EINT6/SEG30
LCDBL1				P37/AN7/EINT7/SEG31
VI0	I	The input of a high gain inverter amplifiers	Input	–
VI1	I/O			P32/EINT2/SEG26
VI2				P34/ENIT4/SEG28
VO0	O	The output of a high gain inverter amplifiers	Output	–
VO1	I/O		Input	P33/EINT3/SEG27
VO2				P35/EINT5/SEG29
VLC0	I/O	LCD bias voltage pins	Input	P50
VLC2				P51
VLC3				P52
CAPH	I/O	Capacitor terminals for voltage booster	Input	P53
CAPL				P54
COM0	I/O	LCD common signal outputs	Input	P55
COM1				P56
COM2				P00/SEG0
COM3				P01/SEG1
COM4				P02/SEG2
COM5				P03/SEG3
COM6				P04/SEG4
COM7				P05/SEG5

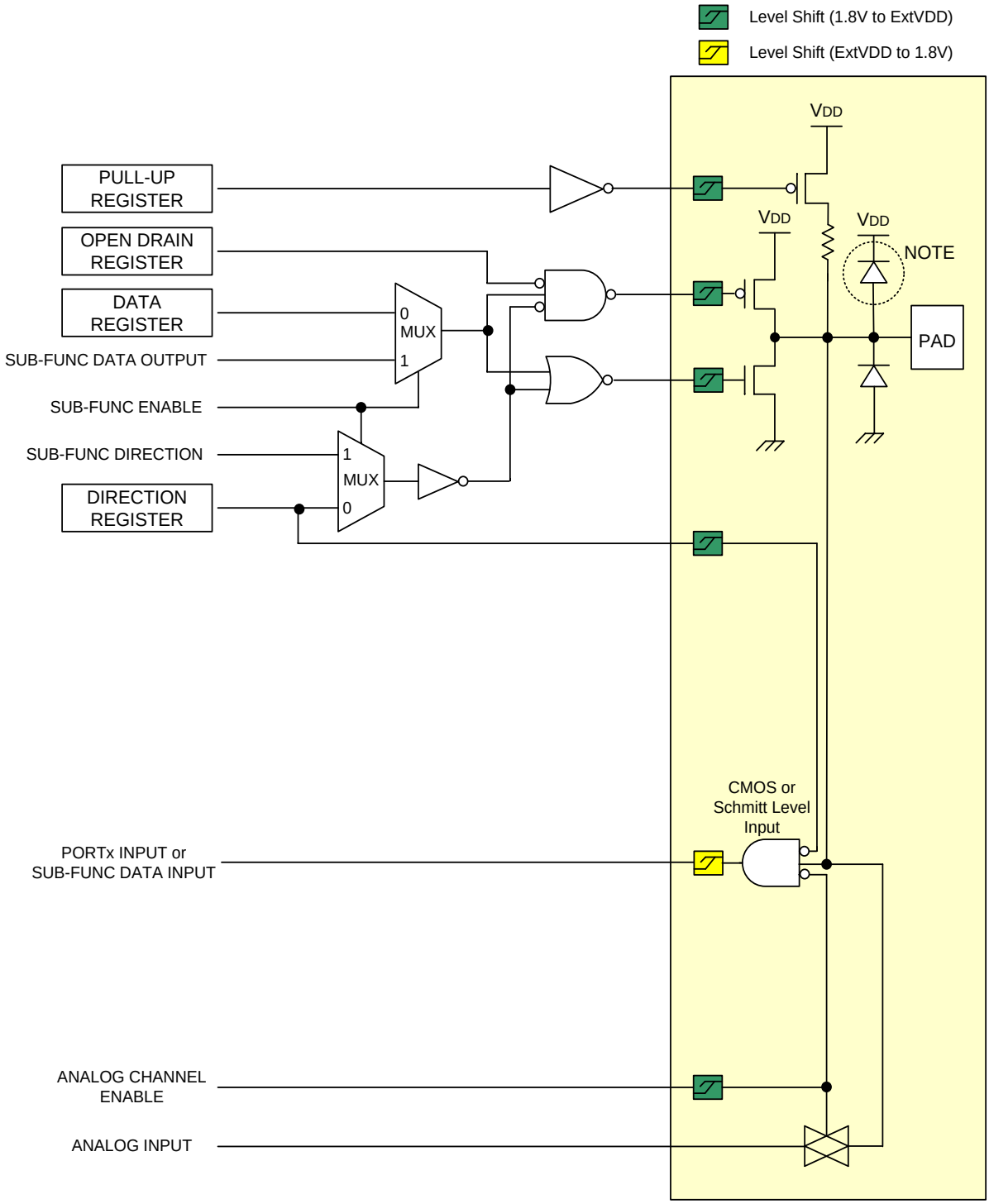
Pin Names	I/O	Pin Description	After RESET	Alternative Functions
SEG0	I/O	LCD segment signal outputs	Input	P00/COM2
SEG1				P01/COM3
SEG2				P02/COM4
SEG3				P03/COM5
SEG4				P04/COM6
SEG5				P05/COM7
SEG6				P06
SEG7				P07
SEG8				P10
SEG9				P11
SEG10				P12
SEG11				P13
SEG12				P14
SEG13				P15
SEG14				P16
SEG15				P17/DSDA
SEG16				P20/DSCL
SEG17				P21
SEG18				P22
SEG19				P23
SEG20				P24
SEG21				P25
SEG22				P26
SEG23				P27
SEG24				P30/EINT0
SEG25				P31/EINT1
SEG26				P32/EINT2
SEG27				P33/EINT3
SEG28				P34/EINT4
SEG29				P35/EINT5
SEG30				P36/EINT6
SEG31				P37/EINT7

Pin Names	I/O	Pin Description	After RESET	Alternative Functions
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION”	Input	P42/AN2/EC2
DSDA	I/O	On chip debugger data input/output	Input	P17/SEG15
DSCL	I/O	On chip debugger clock input	Input	P20/SEG16
XIN	I/O	Main oscillator pins	Input	P40/AN0/EINT13/T3O/PWM3O
XOUT				P41/AN1/EINT12/T2O/PWM2O
SXIN	I/O	Sub oscillator pins	Input	P44/AN4
SXOUT				P45/AN5
VREG	I/O	Regulator voltage output for sub clock 0.1uF capacitor needed	Input	P43/AN3
VDD, VSS	–	Power input pins	–	–

Notes: 1. The P42/RESETB pin is configured as one of P42 and RESETB pin by the “CONFIGURE OPTION”.
2. The P40/XIN and P41/XOUT pins are configured as a function pin by software control.
3. The P44/SXIN, P45/SXOUT, and P43/VREG pins are configured as a function pin by s/w control.
4. If the P17/SEG15/DSDA and P20/SEG16/DSCL pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
5. The P17/SEG15/DSDA and P20/SEG16/DSCL pins are configured as inputs with internal pull-up resistors only during the reset or power-on reset.

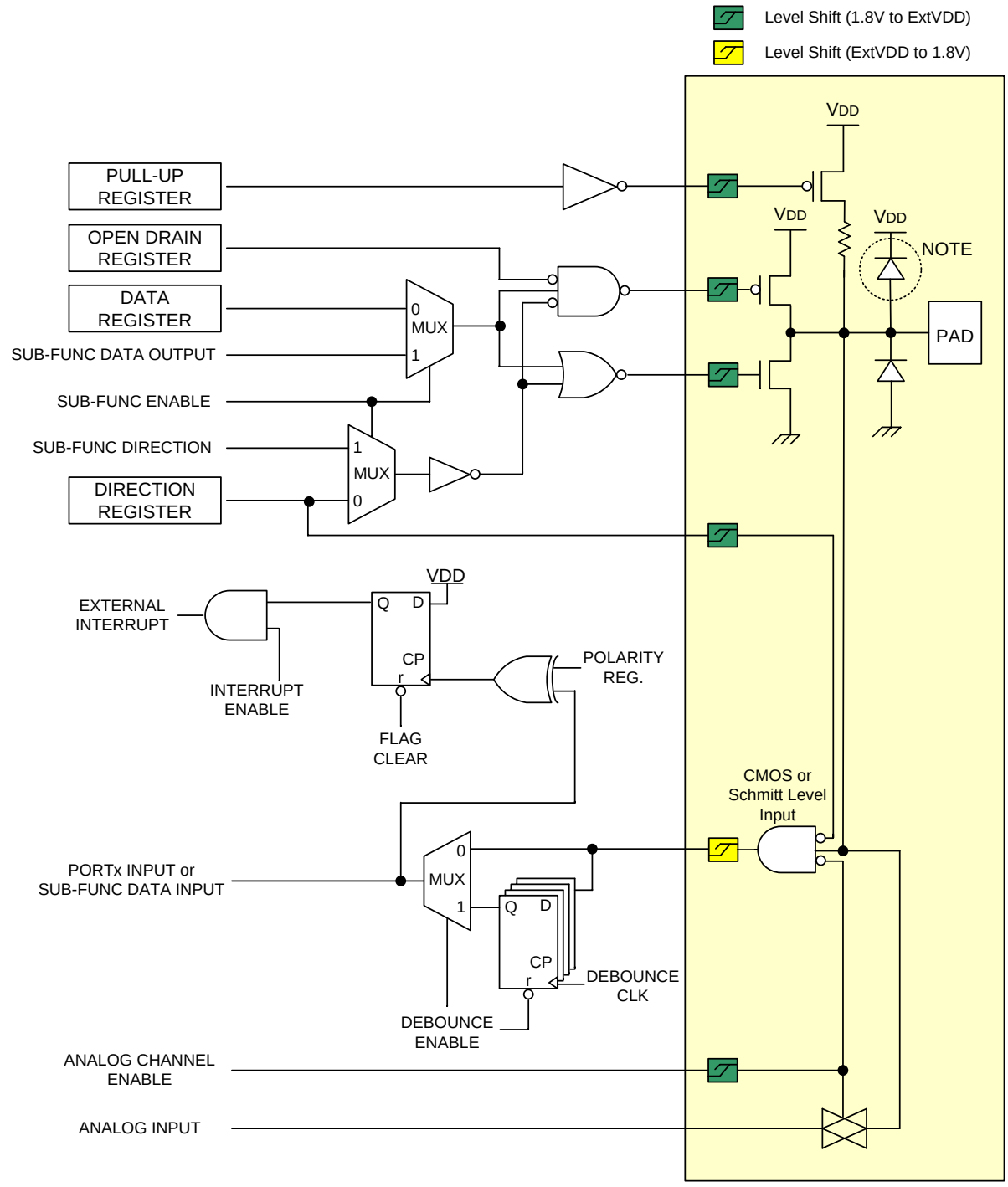
5. PORT STRUCTURES

5.1 GENERAL PURPOSE I/O PORT



Note)
The P0, P1, P2, P3, and P5 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

5.2 EXTERNAL INTERRUPT I/O PORT



Note)
The P0, P1, P2, P3, and P5 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	V_{DD}	-0.3 – +4.0	V	–
Normal Pin	V_I	-0.3 – V_{DD}+0.3	V	Voltage on any pin with respect to Vss
	V_O	-0.3 – V_{DD}+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-80	mA	Maximum current (ΣI_{OH})
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	120	mA	Maximum current (ΣI_{OL})
REM Output Pin	I_{OL}	800	mA	Maximum current sunk by REM pin
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 – +150	°C	–

6.2 RECOMMENDED OPERATING CONDITIONS

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions			Min	Max	Units
Operating Voltage	V_{DD}	fx = 32 – 38kHz	SX-tal		1.8	3.6	V
		fx = 0.4 – 4.2MHz	X-tal,	Ceramic	1.8	3.6	
				Crystal	2.0	3.6	
		fx = 0.4 – 8MHz	X-tal		2.4	3.6	
		fx = 0.4 – 12MHz			3.0	3.6	
		fx = 0.5 – 8MHz	HFIRC		1.8	3.6	
		fx = 4.0 – 32kHz	LFIRC		1.8	3.6	
Operating Temperature	T_{OPR}	V_{DD} = 1.8 – 3.6V			-40	85	°C

6.3 A/D CONVERTER CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	10	–	bit
Integral Non-Linear Error	INL	VDD=2.4V – 3.6V, fx=8MHz		–	–	±3	LSB
Differential Non-Linearity Error	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	tCON	VDD=2.4V – 3.6V		30	–	–	us
		VDD=2.7V – 3.6V		20	–	–	
Analog Input Voltage	VAN	–		VSS	–	VDD	V
Band Gap Reference Value(4)	VAL_{BGR}	VDD=3.3V, TA=25℃, MSB align, 8 times average, Different from CNFMRR0/1 values and ADC result (“CNFMRR0/1” – “ADC result”)		–	–	±15	LSB
A/DC Input Leakage Current	IAN	VDD=3.072V		–	–	10	uA
A/DC Current	IADC	Enable	VDD=3.072V	–	1	2	mA
		Disable		–	–	0.1	uA

Notes:
1. Zero offset error is the difference between 0x000 and the converted output for zero input voltage(VSS);
2. Full scale error is the difference between 0x3ff and the converted output for full-scale input voltage(VDD).
3. If VDD is less than 2.4V, the resolution degrades by 1-bit whenever VDD drops 0.1V. (@ADCLK = 0.5MHz, under 2.7V resolution has no test.)
4. The CNFMRR0/1 register of XRAM has an AD/C result value which reads V_{BGR} voltage at VDD=3.3V. The CNFMRR0 has the value of ADCDRL[7:0] and CNFMRR1 has the value of ADCDRH[7:0].

6.4 POWER-ON RESET CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Release Level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.2	–	V
V_{DD} Voltage Rising Time	tR	0.5V to 2V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

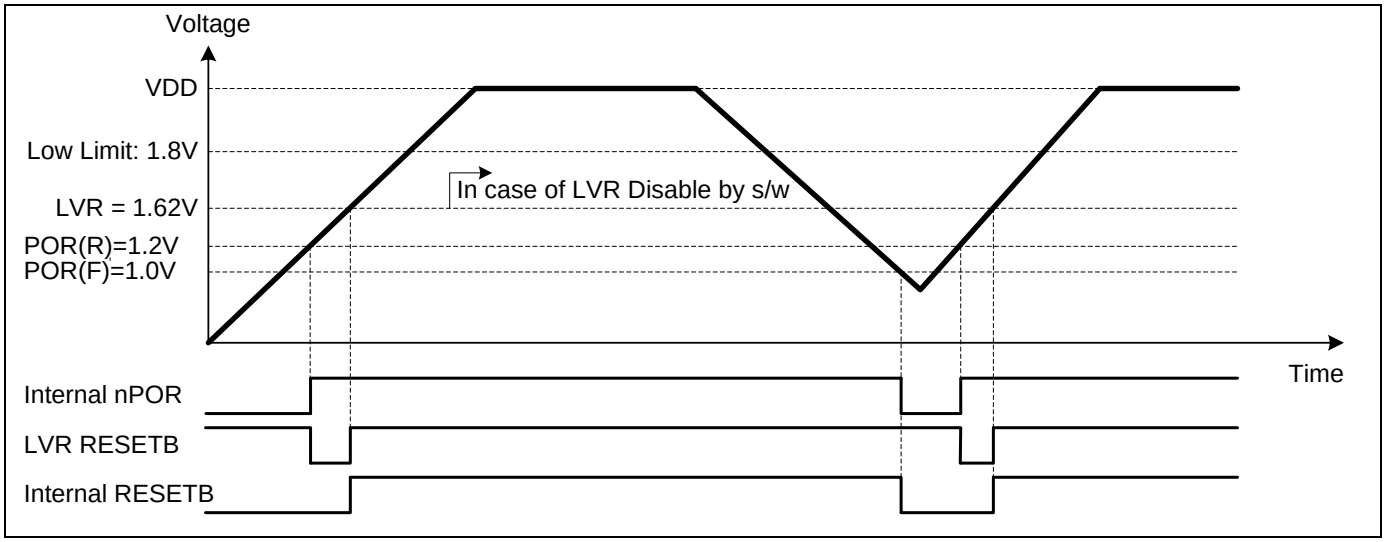


Figure 6–1. POR Timing

6.5 HIGH FREQUENCY INTERNAL RC OSCILLATOR CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{HFIRC}	VDD=1.8V – 3.6V		–	8	–	MHz
Tolerance	–	T_A = -10 °C to + 55°C	With 0.1uF bypass capacitor	–	–	±2.0	%
		T_A = - 20 °C to + 85°C				±3.0	
		T_A = - 40 °C to + 85°C				±4.0	
		T_A = -10 °C to + 55°C 1. User trim by E-PGM+ only. 2. User trim by S/W.				±1.0	
Clock duty ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{HFS}	–		–	–	100	us
HFIRC Current	I_{HFIRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Notes: 1. User Trimming means the calibration of HFIRC frequency. Using E-PGM +.
2. To ensure ±1.0% tolerance of HFIRC frequency, it is necessary to do User Trimming.
3. Guaranteed by design, but might be On-Board programming after SMT process.
(HFIRC Calibration with high temperature can cause the shift of the frequency, be sure to calibrate Enough to cool to near room temperature after SMT process)

6.6 LOW FREQUENCY INTERNAL RC OSCILLATOR CHARACTERISTICS

(T_A = - 40°C to + 85°C, VDD = 1.8 – 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{LFIRC}	VDD=1.8V – 3.6V		–	32	–	kHz
Tolerance	–	T_A = - 10 °C to + 55°C	With 0.1uF bypass capacitor	–	–	±10.0	%
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{LFS}	–		–	–	1	ms
LFIRC Current	I_{LFIRC}	Enable	VDD=3.0V	–	5	–	uA
		Disable		–	–	0.1	

6.7 LOW VOLTAGE RESET AND LOW VOLTAGE INDICATOR CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.62V.		–	1.62	1.79	V
				1.85	2.00	2.15	
				2.25	2.40	2.55	
				2.53	2.68	2.83	
LVR Hysteresis	△V	–		–	50	150	mV
LVI Hysteresis	△V	–		–	10	50	
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	V_{DD}=3V RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)		–	–	0.1	

6.8 INTERNAL WATCH-DOG TIMER RC OSCILLATOR CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

6.9 LCD VOLTAGE CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 2.0 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LCD Voltage	VLC3	Voltage booster enabled, 1/2 bias	Typx0.93	1.0+(Nx0.05)	Typx1.07	V
		Voltage booster enabled, 1/3 bias	Typx0.93	0.75	Typx1.07	
				0.79		
				0.83		
				0.86		
				0.90		
				0.94		
				0.98		
				1.01		
				1.05		
				1.09		
LCD Mid Bias Voltage	VLC0/2	Voltage booster enabled, 1/2 bias, No panel load, VDD=3V	Typx0.9	2xVLC3	Typx1.1	V
	VLC0	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V	Typx0.9	3xVLC3	Typx1.1	
	VLC2		Typx0.9	2xVLC3	Typx1.1	
	VLC2	Voltage booster disabled, LCD dividing resistor, VDD=2.7V to 3.6V, 1/3 bias, LCD clock = 0Hz, VLC0=VDD	Typ-0.2	0.67xVDD	Typ+0.2	V
	VLC3		Typ-0.2	0.33xVDD	Typ+0.2	
LCD Driver Output Impedance	R_{LO}	VLCD=3V, ILOAD=±10uA	–	5	10	kΩ
LCD Bias Dividing Resistor	R_{LCD1}	Internal resistor mode, T_A = 25°C	20	30	40	kΩ
	R_{LCD2}		40	60	80	
	R_{LCD3}		80	120	160	
LCD Block Current	I_{LCD}	Voltage booster mode, VDD=3V, VLCD=3.15V, 1/3Bias	–	3	6	uA

Note: Where N is the value of LCDCCR register (N = 0 to 9).

6.10 DC ELECTRICAL CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V, fx=12MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	VIH1	P17, P20, P3, P4, RESETB		0.8VDD	–	VDD	V
	VIH2	All input pins except VIH1		0.7VDD	–	VDD	
Input Low Voltage	VIL1	P17, P20 P3, P4, RESETB		–	–	0.2VDD	V
	VIL2	All input pins except VIL1		–	–	0.3VDD	
Output High Voltage	VOH	VDD=3.3V, IOH = – 2mA; All output ports except REM pin		VDD-1.0	–	–	V
Output Low Voltage	VOL1	VDD=3.3V, IOL=10mA; All output ports except VOL2 and REM		–	–	1.0	V
	VOL2	VDD=3.0V, LCDBL0 and LCDBL1	IOL=10mA, DRV = 0	–	–	1.0	V
			IOL=20mA, DRV = 1				
			IOL=30mA, DRV = 2				
Inverter Amp Output Current	IOHA	VDD=3V, VOH=2.5V VO0, VO1, and VO2		-700	-400	-200	uA
	IOLA	VDD=3V, VOL=0.5V VO0, VO1, and VO2		200	400	700	
REM Output High Current	IOHR	VDD=3.0V, VOH=2.0V, ROTS=1		–	-10	-5	mA
REM Output Low Current	IOL1	VDD=3.0V, VOL=1.0V, TA=25°C	ROTS=1	2.5	5.0	–	mA
	IOL2		ROTS=0, RIOL=3	470	630	–	
Input high leakage current	IIH	All Input ports		–	–	1	uA
Input low leakage current	IIL	All Input ports		– 1	–	–	uA
Pull-up resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=3V	50	100	150	kΩ
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=3V	200	400	600	
OSC feedback resistor	RX1	XIN=VDD, XOUT=VSS TA=25°C, VDD=3V FBS = 0 (Configure Option 2: 1FH)		1200	2400	3500	kΩ
		XIN=VDD, XOUT=VSS TA=25°C, VDD=3V FBS = 1 (Configure Option 2: 1FH)		500	1000	1500	kΩ
	RX2	SXIN=VDD, SXOUT=VSS TA=25°C, VDD=3V		5	10	20	MΩ

6.11 DC ELECTRICAL CHARACTERISTICS (CONTINUED)

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V, fx=12MHz)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current	IDD1 (Run)	fxin=12MHz, VDD=3V±10%	–	2.5	5.0	mA
		HFIRC=8MHz, VDD=3V±10%	–	2.0	4.0	
		fxin=8MHz, VDD=3V±10%	–	2.0	4.0	
	IDD2 (Idle)	fxin=12MHz, VDD=3V±10%	–	1.5	3.0	mA
		HFIRC=8MHz, VDD=3V±10%	–	0.7	1.4	
		fxin=8MHz, VDD=3V±10%	–	1.0	2.0	
	IDD3 (Run)	fsub=32.768kHz, VDD=3V±10%, TA=25°C	–	90.0	180.0	uA
		LFIRC=32kHz, VDD=3V±10% TA=25°C	–	90.0	180.0	
	IDD4 (Idle)	fsub=32.768kHz, VDD=3V±10%, TA=25°C	–	4.0	8.0	uA
		LFIRC=32kHz, VDD=3V±10% TA=25°C		6.0	12.0	
	IDD5	Stop, VDD=3V±10%, TA=25°C	–	0.5	3.0	uA

Notes: 1. Where the fxin is an external main oscillator, the fsub is an external sub oscillator, the HFIRC is an internal high frequency RC oscillator, the LFIRC is an internal low frequency RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal watch-dog timer RC(WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

6.12 AC CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 V to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	V_{DD} = 3 V	10	–	–	us
Interrupt Input High, Low width	t_{IWH}, t_{IWL}	All interrupts, V_{DD} = 3 V	200	–	–	ns
REM port High, Low width	t_{REMWH}, t_{REMWL}	REM, V_{DD} = 3 V	5	–	–	us

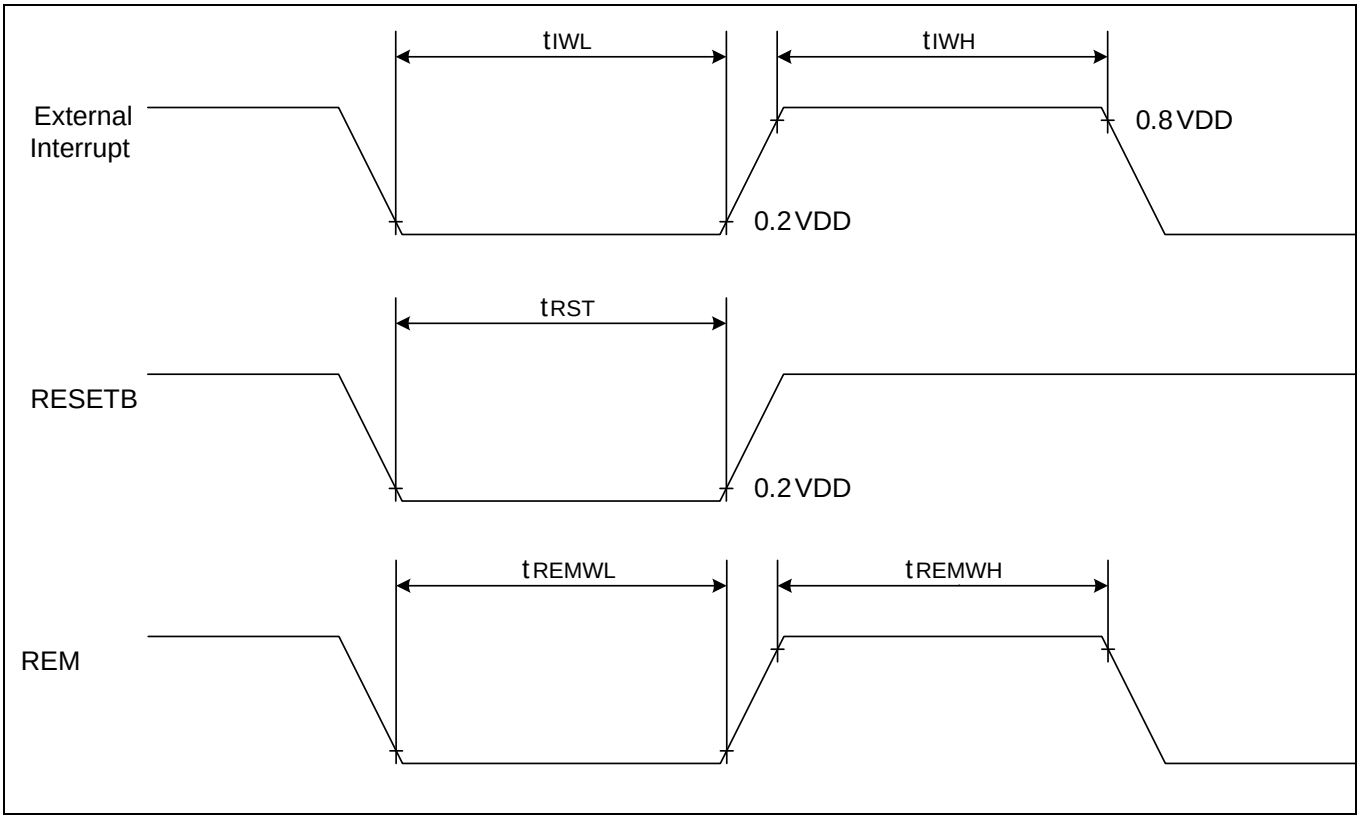
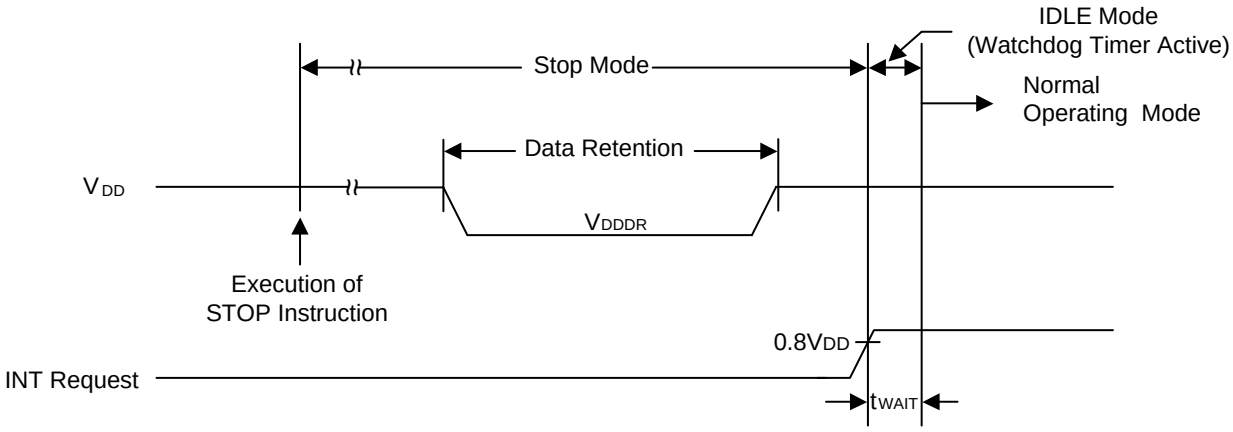


Figure 6–2. AC Timing

6.13 DATA RETENTION VOLTAGE IN STOP MODE

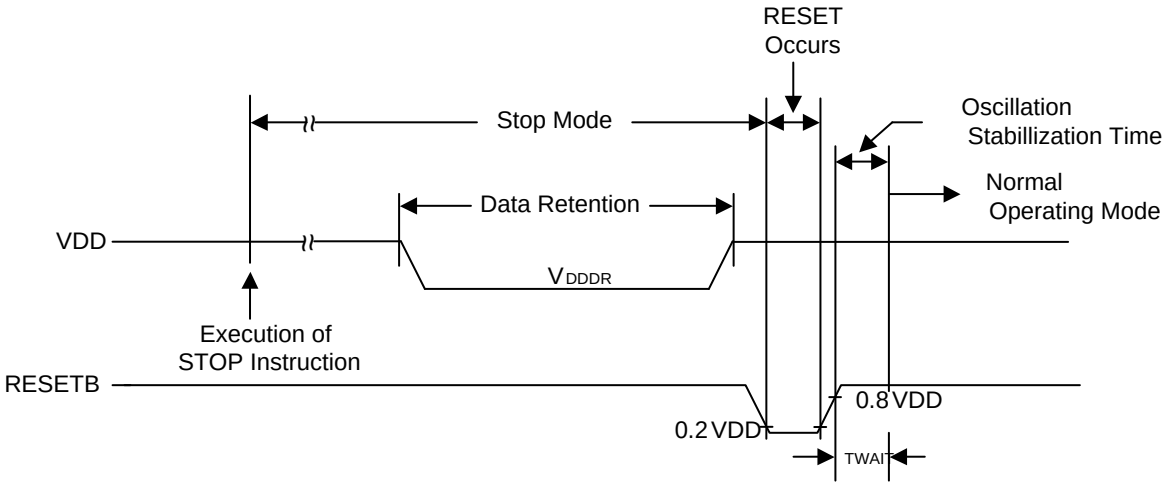
(T_A = - 40°C to + 85°C, V_{DD} = 1.8 V to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.0	–	3.6	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8V (T_A = 25 °C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 6–3. Stop Mode Release Timing When Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 4/f_{IRC}) = (16.4 mS at fx=1MHz).

Figure 6–4. Stop Mode Release Timing When Initiated by RESETB

6.14 INTERNAL FLASH ROM CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 – 3.6V, Vss=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sector Write Time	TFSW	–	–	2.5	2.7	ms
Sector Erase Time	TFSE	–	–	3.0	3.2	
Hard-Lock Time	TFHL	–	–	2.5	2.7	
Page Buffer Reset Time	TFBR	–	–	–	5	us
Flash Programming Frequency	fPGM	–	0.4	–	–	MHz
Endurance of Write/Erase (Sector 0~375)	NFWE	TA = 25°C	–	–	10,000	Times
Endurance of Write/Erase (Sector 376~383)			–	–	100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

6.15 INPUT/OUTPUT CAPACITANCE

(T_A = - 40°C to + 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	CIN	f=1MHz Unmeasured pins are connected to Vss	–	–	10	pF
Output Capacitance	COUT					
I/O Capacitance	CIO					

6.16 MAIN OSCILLATOR CHARACTERISTICS

(T_A = - 40°C to + 85°C, V_{DD} = 1.8 V to 3.6 V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Main oscillation frequency	2.0 V – 3.6 V	0.4	–	4.2	MHz
		2.4 V – 3.6 V	0.4	–	8.0	
		3.0 V – 3.6 V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8 V – 3.6 V	0.4	–	4.2	
		2.4 V – 3.6 V	0.4	–	8.0	
		3.0 V – 3.6 V	0.4	–	12.0	
External Clock	XIN input frequency	1.8 V – 3.6 V	0.4	–	4.2	MHz
		2.4 V – 3.6 V	0.4	–	8.0	
		3.0 V – 3.6 V	0.4	–	12.0	

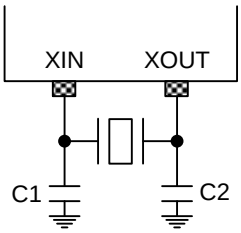


Figure 6–5. Crystal/Ceramic Oscillator

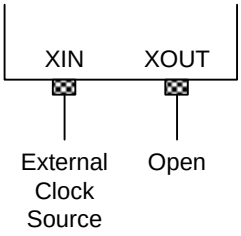


Figure 6–6. External Clock

6.17 SUB OSCILLATOR CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 3.6 V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 3.6 V	32	32.768	38	kHz

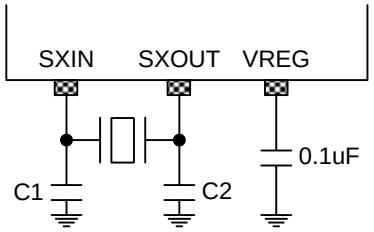


Figure 6–7. Crystal Oscillator

6.18 MAIN OSCILLATION STABILIZATION TIME

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 3.6 V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	f_{XIN} ≥ 1 MHz, VDD = 2.0V~3.6V Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic	f_{XIN} ≥ 1 MHz, VDD = 1.8V~3.6V Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	
External Clock	f_{XIN} = 0.4 to 12 MHz XIN input high and low width (t_{XL}, t_{XH})	42	–	1250	ns

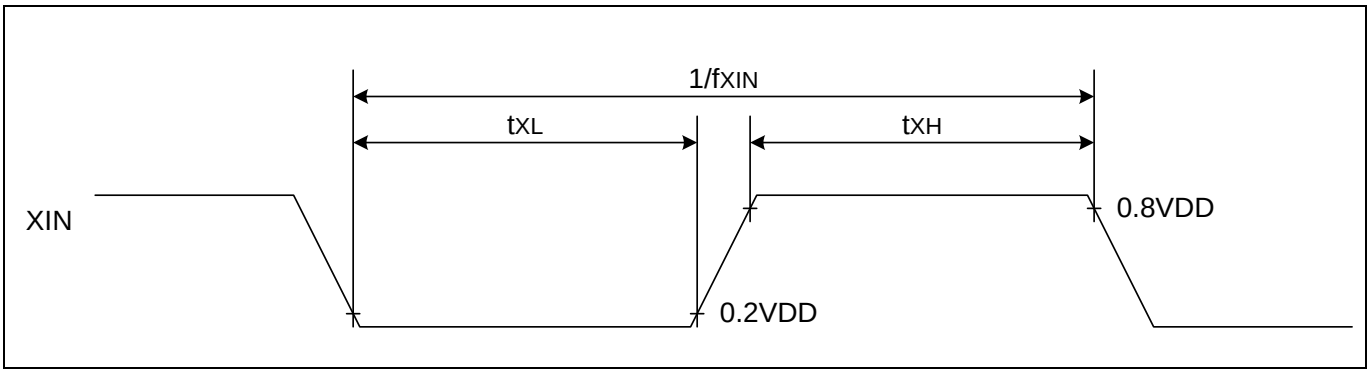


Figure 6–8. Clock Timing Measurement at XIN

6.19 SUB OSCILLATION STABILIZATION TIME

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 3.6 V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD = 3.0V, T_A = 25°C	–	0.7	1.5	
External Clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	us

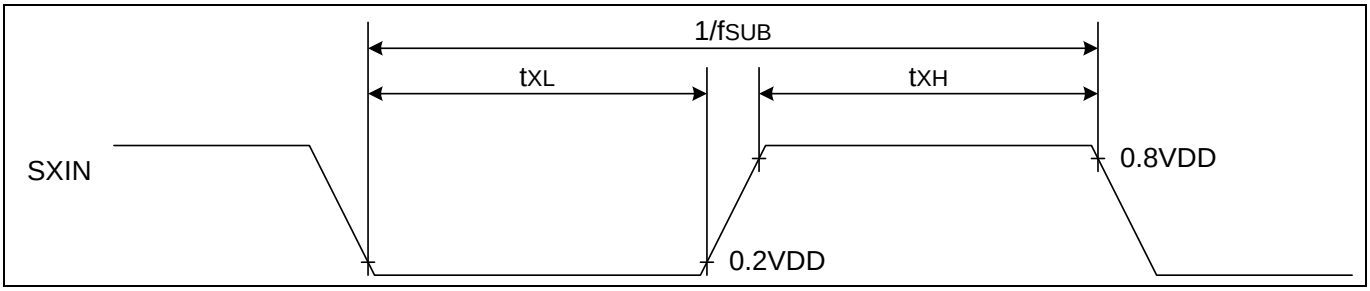


Figure 6–9. Clock Timing Measurement at SXIN

6.20 OPERATING VOLTAGE RANGE

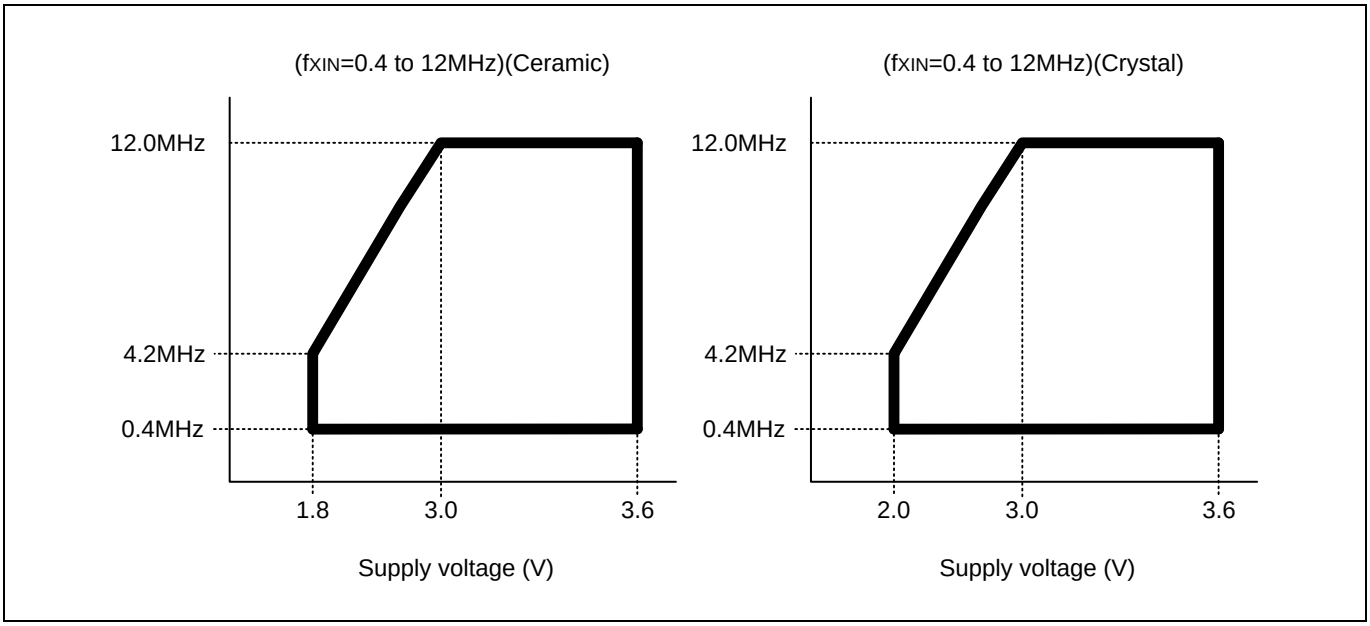


Figure 6–10. Operating Voltage Range (Main)

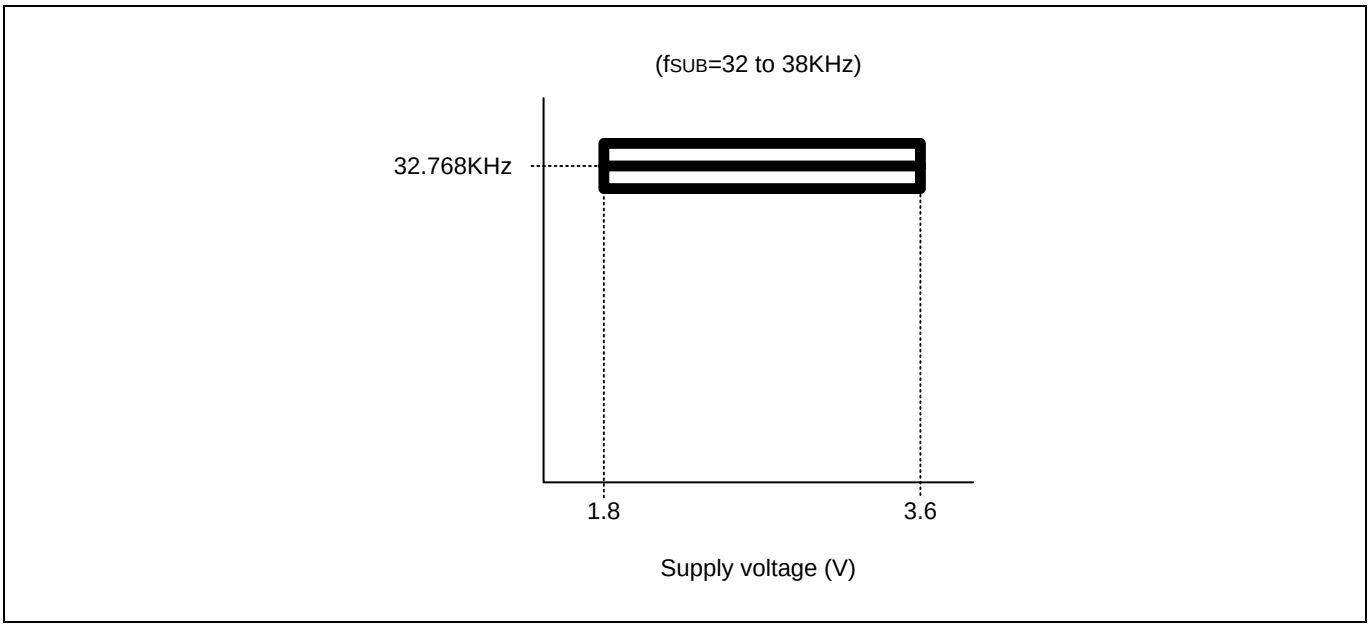
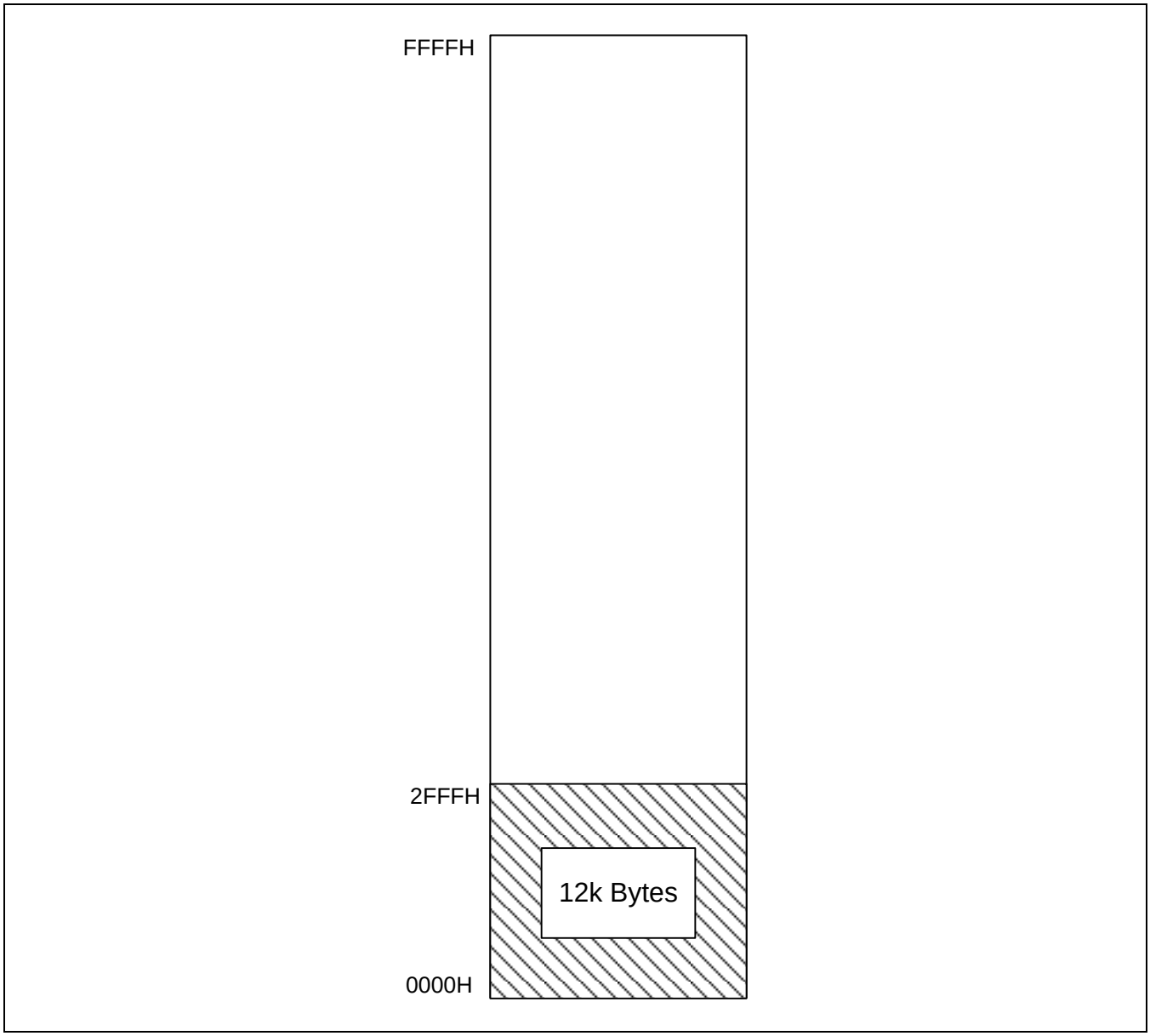


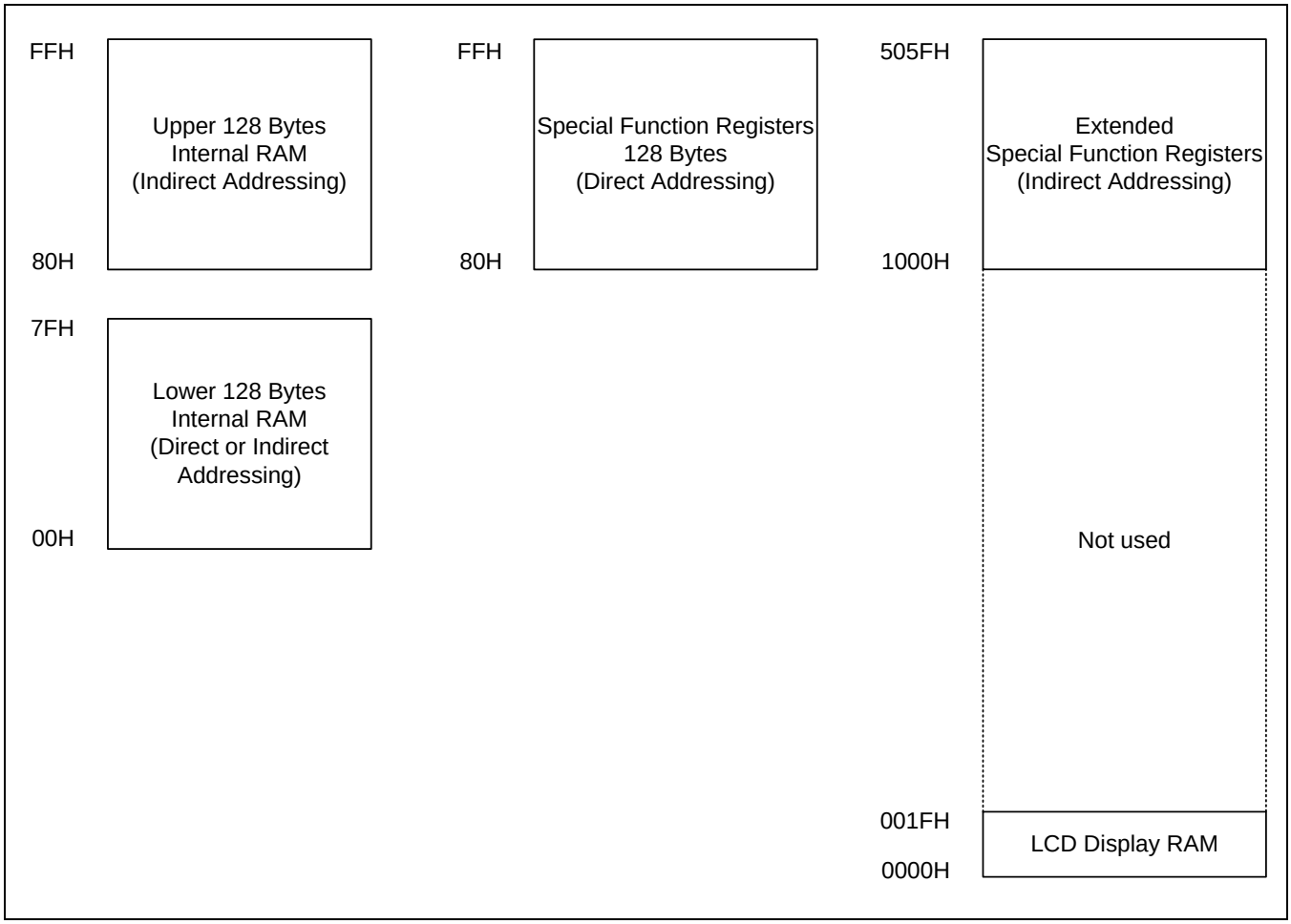
Figure 6–11. Operating Voltage Range (Sub)

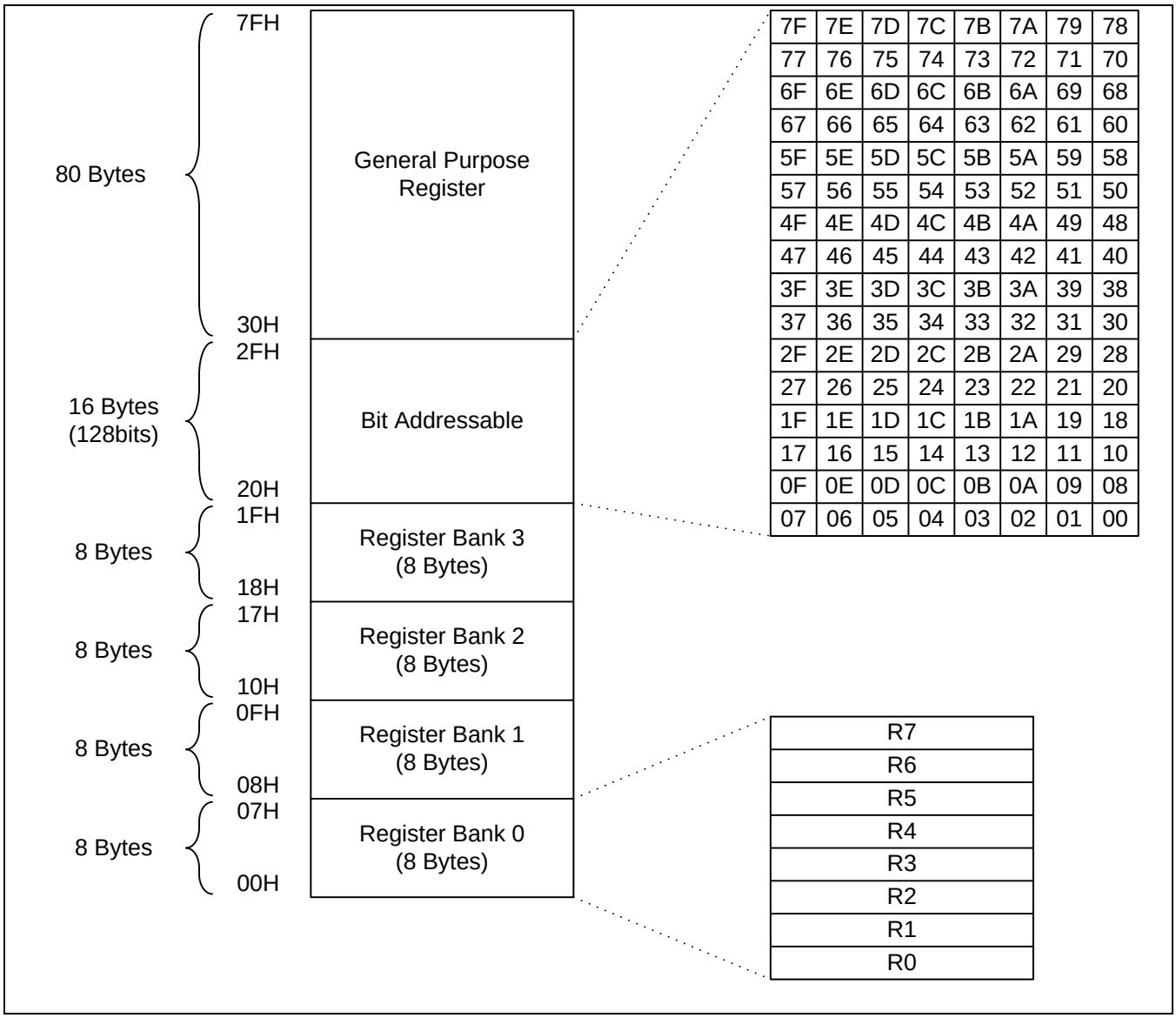
7. MEMORY

7.1 PROGRAM MEMORY



7.2 DATA MEMORY





Lower 128 bytes RAM

7.3 SFR MAP

7.3.1 SFR MAP SUMMARY

Reserved

M8051 Compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1		FSADRH	FSADRM	FSADRL	FIDR	FMCR	
0F0H	B	P5FSR						
0E8H	RSTFR	P0FSR	P1FSR	P2FSR	P3FSRL	P3FSRH	P4FSRL	P4FSRH
0E0H	ACC	IAMPCR						IRCIDR
0D8H	LVRCR		P0PU	P1PU	P2PU	P3PU	P4PU	P5PU
0D0H	PSW	P5IO	P0OD	P1OD	P2OD	P3OD	P4OD	P5OD
0C8H	OSCCR	P4IO	T3CRL	T3CRH	T3ADRL	T3ADRH	T3BDRL	T3BDRH
0C0H		P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CR	T1CNT	T1DRL	T1DRH	CARCR	LIFSR
0B0H	P5	P1IO	T0CR	T0CNT	T0DR	ITCRL	ITCRH	
0A8H	IE	IE1	IE2	IE3		ITDRL	ITDRH	FCDIN
0A0H	P4	P0IO	EO	EIFLAG0	EIPOL0	EIFLAG1	EIPOL1L	EIPOL1H
98H	P3	LCDCRL	LCDCRH	LCDCCR	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	LCDBLCR			P3DB	P4DB	WTCR	IRCTRM
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	IRCTCR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

Notes: 1. (1) These registers are bit-addressable

7.3.2 EXTENDED SFR MAP SUMMARY

☐ Reserved

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
5058H	FCDRL							
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH
1078H								
1070H	CNFMRR0	CNFMRR1	CNFMRR2	CNFMRR3				

7.3.3 SFR MAP

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
P0 Data Register	P0	80H	R/W	0	0	0	0	0	0	0	0
Stack Pointer	SP	81H	R/W	0	0	0	0	0	1	1	1
Data Pointer Register Low	DPL	82H	R/W	0	0	0	0	0	0	0	0
Data Pointer Register High	DPH	83H	R/W	0	0	0	0	0	0	0	0
Data Pointer Register Low 1	DPL1	84H	R/W	0	0	0	0	0	0	0	0
Data Pointer Register High 1	DPH1	85H	R/W	0	0	0	0	0	0	0	0
Low Voltage Indicator Control Register	LVICR	86H	R/W	–	–	0	0	–	–	0	0
Power Control Register	PCON	87H	R/W	0	–	–	–	0	0	0	0
P1 Data Register	P1	88H	R/W	0	0	0	0	0	0	0	0
Watch Timer Data Register	WTDR	89H	W	0	1	1	1	1	1	1	1
Watch Timer Counter Register	WTCNT	89H	R	–	0	0	0	0	0	0	0
System and Clock Control Register	SCCR	8AH	R/W	–	–	–	–	–	–	0	0
BIT Control Register	BITCR	8BH	R/W	0	0	0	–	0	0	0	1
Basic Interval Timer Counter Register	BITCNT	8CH	R	0	0	0	0	0	0	0	0
Watch Dog Timer Control Register	WDTCR	8DH	R/W	0	0	0	–	–	–	0	0
Watch Dog Timer Data Register	WDTDR	8EH	W	1	1	1	1	1	1	1	1
Watch Dog Timer Counter Register	WDTCNT	8EH	R	0	0	0	0	0	0	0	0
Internal RC Trim Control Register	IRCTCR	8FH	R/W	0	0	0	0	0	0	0	0
P2 Data Register	P2	90H	R/W	0	0	0	0	0	0	0	0
LCD Back Light Control Register	LCDBLCR	91H	R/W	–	–	–	–	0	0	0	0
Reserved		92H	–								
Reserved		93H	–								
P3 Debounce Enable Register	P3DB	94H	R/W	0	0	0	0	0	0	0	0
P4 Debounce Enable Register	P4DB	95H	R/W	0	0	–	–	–	–	0	0
Watch Timer Control Register	WTCR	96H	R/W	0	–	0	0	0	0	0	0
Internal RC Trim Register	IRCTRM	97H	R/W	x	x	x	x	x	x	x	x
P3 Data Register	P3	98H	R/W	0	0	0	0	0	0	0	0
LCD Driver Control Low Register	LCDCRL	99H	R/W	0	0	–	0	0	0	0	0
LCD Driver Control High Register	LCDCRH	9AH	R/W	–	–	–	–	–	0	0	0
LCD Contrast Control Register	LCDCCR	9BH	R/W	–	–	–	–	0	0	0	0
A/D Converter Control Low Register	ADCCRL	9CH	R/W	0	0	–	0	0	0	0	0
A/D Converter Control High Register	ADCCRH	9DH	R/W	0	–	–	–	–	0	0	0
A/D Converter Data Low Register	ADCDRL	9EH	R	x	x	x	x	x	x	x	x
A/D Converter Data High Register	ADCDRH	9FH	R	x	x	x	x	x	x	x	x

7.3.3 SFR MAP (CONTINED)

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
P4 Data Register	P4	A0H	R/W	–	–	0	0	0	0	0	0
P0 Direction Register	P0IO	A1H	R/W	0	0	0	0	0	0	0	0
Extended Operation Register	EO	A2H	R/W	–	–	–	0	–	0	0	0
External Interrupt Flag 0 Register	EIFLAG0	A3H	R/W	–	–	–	–	–	0	0	–
External Interrupt Polarity 0 Register	EIPOL0	A4H	R/W	–	–	0	0	0	0	–	–
External Interrupt Flag 1 Register	EIFLAG1	A5H	R/W	0	0	0	0	0	0	0	0
External Interrupt Polarity 1 Low Register	EIPOL1L	A6H	R/W	0	0	0	0	0	0	0	0
External Interrupt Polarity 1 High Register	EIPOL1H	A7H	R/W	0	0	0	0	0	0	0	0
Interrupt Enable Register	IE	A8H	R/W	0	–	0	–	0	0	–	–
Interrupt Enable Register 1	IE1	A9H	R/W	–	–	–	–	–	–	–	–
Interrupt Enable Register 2	IE2	AAH	R/W	–	–	0	0	0	0	0	–
Interrupt Enable Register 3	IE3	ABH	R/W	–	–	–	0	0	0	0	0
Reserved		ACH	–								
Interval Timer Data Low Register	ITDRL	ADH	R/W	1	1	1	1	1	1	1	1
Interval Timer Data High Register	ITDRH	AEH	R/W	1	1	1	1	1	1	1	1
Flash CRC Data In Register	FCDIN	AFH	R/W	0	0	0	0	0	0	0	0
P5 Data Register	P5	B0H	R/W	–	0	0	0	0	0	0	0
P1 Direction Register	P1IO	B1H	R/W	0	0	0	0	0	0	0	0
Timer 0 Control Register	T0CR	B2H	R/W	0	0	–	–	0	0	0	0
Timer 0 Counter Register	T0CNT	B3H	R	0	0	0	0	0	0	0	0
Timer 0 Data Register	T0DR	B4H	R/W	1	1	1	1	1	1	1	1
Interval Timer Control Low Register	ITCRL	B5H	R/W	0	0	0	0	0	–	0	0
Interval Timer Control High Register	ITCRH	B6H	R/W	0	–	–	–	–	–	0	0
Reserved		B7H	–								
Interrupt Priority Register	IP	B8H	R/W	–	–	0	0	0	0	0	0
P2 Direction Register	P2IO	B9H	R/W	0	0	0	0	0	0	0	0
Timer 1 Control Register	T1CR	BAH	R/W	0	0	–	0	0	0	0	0
Timer 1 Counter Register	T1CNT	BBH	R	0	0	0	0	0	0	0	0
Timer 1 Data Low Register	T1DRL	BCH	R/W	1	1	1	1	1	1	1	1
Timer 1 Data High Register	T1DRH	BDH	R/W	1	1	1	1	1	1	1	1
Carrier Control Register	CARCR	BEH	R/W	0	0	0	0	0	0	0	0
LFIRC Frequency Selection Register	LIFSR	BFH	R/W	0	0	0	0	0	–	0	0

7.3.3 SFR MAP (CONTINED)

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
Reserved		C0H	–								
P3 Direction Register	P3IO	C1H	R/W	0	0	0	0	0	0	0	0
Timer 2 Control Low Register	T2CRL	C2H	R/W	0	0	0	0	0	0	0	0
Timer 2 Control High Register	T2CRH	C3H	R/W	0	–	0	0	0	–	0	0
Timer 2 A Data Low Register	T2ADRL	C4H	R/W	1	1	1	1	1	1	1	1
Timer 2 A Data High Register	T2ADRH	C5H	R/W	1	1	1	1	1	1	1	1
Timer 2 B Data Low Register	T2BDRL	C6H	R/W	1	1	1	1	1	1	1	1
Timer 2 B Data High Register	T2BDRH	C7H	R/W	1	1	1	1	1	1	1	1
Oscillator Control Register	OSCCR	C8H	R/W	0	–	0	0	1	0	0	0
P4 Direction Register	P4IO	C9H	R/W	–	–	0	0	0	0	0	0
Timer 3 Control Low Register	T3CRL	CAH	R/W	0	0	0	0	0	0	–	0
Timer 3 Control High Register	T3CRH	CBH	R/W	0	–	0	0	0	–	0	0
Timer 3 A Data Low Register	T3ADRL	CCH	R/W	1	1	1	1	1	1	1	1
Timer 3 A Data High Register	T3ADRH	CDH	R/W	1	1	1	1	1	1	1	1
Timer 3 B Data Low Register	T3BDRL	CEH	R/W	1	1	1	1	1	1	1	1
Timer 3 B Data High Register	T3BDRH	CFH	R/W	1	1	1	1	1	1	1	1
Program Status Word Register	PSW	D0H	R/W	0	0	0	0	0	0	0	0
P5 Direction Register	P5IO	D1H	R/W	–	0	0	0	0	0	0	0
P0 Open-drain Selection Register	P0OD	D2H	R/W	0	0	0	0	0	0	0	0
P1 Open-drain Selection Register	P1OD	D3H	R/W	0	0	0	0	0	0	0	0
P2 Open-drain Selection Register	P2OD	D4H	R/W	0	0	0	0	0	0	0	0
P3 Open-drain Selection Register	P3OD	D5H	R/W	0	0	0	0	0	0	0	0
P4 Open-drain Selection Register	P4OD	D6H	R/W	–	–	0	0	0	0	0	0
P5 Open-drain Selection Register	P5OD	D7H	R/W	–	0	0	0	0	0	0	0
Low Voltage Reset Control Register	LVRCR	D8H	R/W	0	–	–	0	–	–	0	0
Reserved		D9H	–								
P0 Pull-up Resistor Selection Register	P0PU	DAH	R/W	0	0	0	0	0	0	0	0
P1 Pull-up Resistor Selection Register	P1PU	DBH	R/W	0	0	0	0	0	0	0	0
P2 Pull-up Resistor Selection Register	P2PU	DCH	R/W	0	0	0	0	0	0	0	0
P3 Pull-up Resistor Selection Register	P3PU	DDH	R/W	0	0	0	0	0	0	0	0
P4 Pull-up Resistor Selection Register	P4PU	DEH	R/W	–	–	0	0	0	0	0	0
P5 Pull-up Resistor Selection Register	P5PU	DFH	R/W	–	0	0	0	0	0	0	0

7.3.3 SFR MAP (CONCLUDED)

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
Accumulator A Register	ACC	E0H	R/W	0	0	0	0	0	0	0	0
Inverter Amplifier Control Register	IAMPCR	E1H	R/W	0	–	0	0	–	–	0	0
Reserved		E2H	–								
Reserved		E3H	–								
Reserved		E4H	–								
Reserved		E5H	–								
Reserved		E6H	–								
Internal RC Trim Identification Register	IRCIDR	E7H	R/W	0	0	0	0	0	0	0	0
Reset Flag Register	RSTFR	E8H	R/W	1	x	0	0	x	–	–	–
Port 0 Function Selection Register	P0FSR	E9H	R/W	0	0	0	0	0	0	0	0
Port 1 Function Selection Register	P1FSR	EAH	R/W	0	0	0	0	0	0	0	0
Port 2 Function Selection Register	P2FSR	EBH	R/W	0	0	0	0	0	0	0	0
Port 3 Function Selection Low Register	P3FSRL	ECH	R/W	0	0	0	0	–	0	–	0
Port 3 Function Selection High Register	P3FSRH	EDH	R/W	0	0	0	0	0	0	0	0
Port 4 Function Selection Low Register	P4FSRL	EEH	R/W	–	–	0	0	0	0	0	0
Port 4 Function Selection High Register	P4FSRH	EFH	R/W	0	0	–	–	–	0	0	0
B Register	B	F0H	R/W	0	0	0	0	0	0	0	0
Port 5 Function Selection Register	P5FSR	F1H	R/W	–	0	0	0	0	0	0	0
Reserved		F2H	–								
Reserved		F3H	–								
Reserved		F4H	–								
Reserved		F5H	–								
Reserved		F6H	–								
Reserved		F7H	–								
Interrupt Priority Register 1	IP1	F8H	R/W	–	–	0	0	0	0	0	0
Reserved		F9H	–								
Flash Sector Address High Register	FSADRH	FAH	R/W	–	–	–	–	0	0	0	0
Flash Sector Address Middle Register	FSADRM	FBH	R/W	0	0	0	0	0	0	0	0
Flash Sector Address Low Register	FSADRL	FCH	R/W	0	0	0	0	0	0	0	0
Flash Identification Register	FIDR	FDH	R/W	0	0	0	0	0	0	0	0
Flash Mode Control Register	FMCR	FEH	R/W	0	–	–	–	–	0	0	0
Reserved		FFH	–								

7.3.4 EXTENDED SFR MAP

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
- - - - - - - - - - - - - - - - - - - -											
Configure Mirror Register 0	CNFMRR0	1070H	R	x	x	x	x	x	x	x	x
Configure Mirror Register 1	CNFMRR1	1071H	R	x	x	x	x	x	x	x	x
Configure Mirror Register 2	CNFMRR2	1072H	R	x	x	x	x	x	x	x	x
Configure Mirror Register 3	CNFMRR3	1073H	R	x	x	x	x	x	x	x	x
- - - - - - - - - - - - - - - - - - - -											
Flash CRC Start Address High Register	FCSARH	5050H	R/W	–	–	–	–	–	–	–	0
Flash CRC End Address High Register	FCEARH	5051H	R/W	–	–	–	–	–	–	–	0
Flash CRC Start Address Middle Register	FCSARM	5052H	R/W	0	0	0	0	0	0	0	0
Flash CRC End Address Middle Register	FCEARM	5053H	R/W	0	0	0	0	0	0	0	0
Flash CRC Start Address Low Register	FCSARL	5054H	R/W	0	0	0	0	–	–	–	–
Flash CRC End Address Low Register	FCEARL	5055H	R/W	0	0	0	0	–	–	–	–
Flash CRC Control Register	FCCR	5056H	R/W	0	0	0	–	0	0	0	0
Flash CRC Data High Register	FCDRH	5057H	R/W	1	1	1	1	1	1	1	1
Flash CRC Data Low Register	FCDRL	5058H	R/W	1	1	1	1	1	1	1	1

Note: The CNFMRR0 to 3 registers are mirror to read 4-bytes of configure area.

7.3.5 COMPILER COMPATIBLE SFR

ACC (Accumulator Register) : E0H

.7	.6	.5	.4	.3	.2	.1	.0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ACC Accumulator

B (B Register) : F0H

.7	.6	.5	.4	.3	.2	.1	.0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

B B Register

SP (Stack Pointer) : 81H

.7	.6	.5	.4	.3	.2	.1	.0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 07H

SP Stack Pointer

DPL (Data Pointer Register Low Byte) : 82H

.7	.6	.5	.4	.3	.2	.1	.0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL Data Pointer Low Byte

DPH (Data Pointer Register High Byte) : 83H

.7	.6	.5	.4	.3	.2	.1	.0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH Data Pointer High Byte

DPL1 (Data Pointer Register 1 Low Byte) : 84H

.7	.6	.5	.4	.3	.2	.1	.0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL1 Data Pointer Low1 Byte

DPH1 (Data Pointer Register 1 High Byte) : 85H

.7	.6	.5	.4	.3	.2	.1	.0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH1 Data Pointer High1 Byte

PSW (Program Status Word) : D0H

.7	.6	.5	.4	.3	.2	.1	.0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

CY Carry Flag

AC Auxiliary Carry Flag

F0 General Purpose User-Definable Flag

RS1 Register Bank Select bit 1

RS0 Register Bank Select bit 0

OV Overflow Flag

F1 User-Definable Flag

P Parity Flag. Set/Clear by hardware each instruction cycle to indicate an odd/even number of ‘1’bits in the accumulator.

EO (Extended Operation Register) : A2H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	TRAP_EN	–	DPSEL2	DPSEL1	DPSEL0
–	–	–	R/W	–	R/W	R/W	R/W

Initial value: 00H

TRAP_EN Select the Instruction (Keep always ‘0’)

0 Select MOVC @(DPTR++), A
1 Select Software TRAP Instruction

DPSEL[2:0] Select Banked Data Pointer Register

DPSEL2	DPSEL1	DPSEL0	description
0	0	0	DPTR0
0	0	1	DPTR1

Reserved

8. I/O Ports

8.1 PORT REGISTER

8.1.1 REGISTER MAP

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	A1H	R/W	00H	P0 Direction Register
P0PU	DAH	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	D2H	R/W	00H	P0 Open-drain Selection Register
P0FSR	E9H	R/W	00H	Port 0 Function Selection Register
P1	88H	R/W	00H	P1 Data Register
P1IO	B1H	R/W	00H	P1 Direction Register
P1PU	DBH	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	D3H	R/W	00H	P1 Open-drain Selection Register
P1FSR	EAH	R/W	00H	Port 1 Function Selection Register
P2	90H	R/W	00H	P2 Data Register
P2IO	B9H	R/W	00H	P2 Direction Register
P2PU	DCH	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	D4H	R/W	00H	P2 Open-drain Selection Register
P2FSR	EBH	R/W	00H	Port 2 Function Selection Register
P3	98H	R/W	00H	P3 Data Register
P3IO	C1H	R/W	00H	P3 Direction Register
P3PU	DDH	R/W	00H	P3 Pull-up Resistor Selection Register
P3OD	D5H	R/W	00H	P3 Open-drain Selection Register
P3DB	94H	R/W	00H	P3 Debounce Enable Register
P3FSRH	EDH	R/W	00H	Port 3 Function Selection High Register
P3FSRL	ECH	R/W	00H	Port 3 Function Selection Low Register
P4	A0H	R/W	00H	P4 Data Register
P4IO	C9H	R/W	00H	P4 Direction Register
P4PU	DEH	R/W	00H	P4 Pull-up Resistor Selection Register
P4OD	D6H	R/W	00H	P4 Open-drain Selection Register
P4DB	95H	R/W	00H	P4 Debounce Enable Register
P4FSRH	EFH	R/W	00H	Port 4 Function Selection High Register
P4FSRL	EEH	R/W	00H	Port 4 Function Selection Low Register
P5	B0H	R/W	00H	P5 Data Register
P5IO	D1H	R/W	00H	P5 Direction Register
P5PU	DFH	R/W	00H	P5 Pull-up Resistor Selection Register
P5OD	D7H	R/W	00H	P5 Open-drain Selection Register
P5FSR	F1H	R/W	00H	Port 5 Function Selection Register

Table 8-1 Register Map

8.2 P0 PORT

8.2.1 REGISTER DESCRIPTION FOR P0

P0 (P0 Data Register) : 80H

.7	.6	.5	.4	.3	.2	.1	.0
P07	P06	P05	P04	P03	P02	P01	P00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P0[7:0] I/O Data

P0IO (P0 Direction Register) : A1H

.7	.6	.5	.4	.3	.2	.1	.0
P07IO	P06IO	P05IO	P04IO	P03IO	P02IO	P01IO	P00IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P0IO[7:0] P0 Data I/O Direction

0 Input

1 Output

P0OD (P0 Open-drain Selection Register) : D2H

.7	.6	.5	.4	.3	.2	.1	.0
P07OD	P06OD	P05OD	P04OD	P03OD	P02OD	P01OD	P00OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P0OD[7:0] Configure Open-drain of P0 Port

0 Push-pull output

1 Open-drain output

P0PU (P0 Pull-up Resistor Selection Register) : DAH

.7	.6	.5	.4	.3	.2	.1	.0
P07PU	P06PU	P05PU	P04PU	P03PU	P02PU	P01PU	P00PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P0PU[7:0] Configure Pull-up Resistor of P0 Port

0 Disable

1 Enable

P0FSR (Port 0 Function Selection Register) : E9H

.7	.6	.5	.4	.3	.2	.1	.0
P0FSR7	P0FSR6	P0FSR5	P0FSR4	P0FSR3	P0FSR2	P0FSR1	P0FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P0FSR7 P07 Function Select
- 0 I/O Port
- 1 SEG7

P0FSR6 P06 Function Select
- 0 I/O Port
- 1 SEG6

P0FSR5 P05 Function Select
- 0 I/O Port
- 1 COM7/SEG5

P0FSR4 P04 Function Select
- 0 I/O Port
- 1 COM6/SEG4

P0FSR3 P03 Function Select
- 0 I/O Port
- 1 COM5/SEG3

P0FSR2 P02 Function Select
- 0 I/O Port
- 1 COM4/SEG2

P0FSR1 P01 Function Select
- 0 I/O Port
- 1 COM3/SEG1

P0FSR0 P00 Function Select
- 0 I/O Port
- 1 COM2/SEG0

Note: The P00 – P05 are automatically configured as common or segment signals according to the duty in the LCDCRL register when the pin is selected as a sub-function.

8.3 P1 PORT

8.3.1 REGISTER DESCRIPTION FOR P1

P1 (P1 Data Register) : 88H

.7	.6	.5	.4	.3	.2	.1	.0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1[7:0] I/O Data

P1IO (P1 Direction Register) : B1H

.7	.6	.5	.4	.3	.2	.1	.0
P17IO	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1IO[7:0] P1 Data I/O Direction

0 Input

1 Output

P1OD (P1 Open-drain Selection Register) : D3H

.7	.6	.5	.4	.3	.2	.1	.0
P17OD	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1OD[7:0] Configure Open-drain of P1 Port

0 Push-pull output

1 Open-drain output

P1PU (P1 Pull-up Resistor Selection Register) : DBH

.7	.6	.5	.4	.3	.2	.1	.0
P17PU	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1PU[7:0] Configure Pull-up Resistor of P1 Port

0 Disable

1 Enable

P1FSR (Port 1 Function Selection Register) : EAH

.7	.6	.5	.4	.3	.2	.1	.0
P1FSR7	P1FSR6	P1FSR5	P1FSR4	P1FSR3	P1FSR2	P1FSR1	P1FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1FSR7 P17 Function Select
0 I/O Port
1 SEG15

P1FSR6 P16 Function Select
0 I/O Port
1 SEG14

P1FSR5 P15 Function Select
0 I/O Port
1 SEG13

P1FSR4 P14 Function Select
0 I/O Port
1 SEG12

P1FSR3 P13 Function Select
0 I/O Port
1 SEG11

P1FSR2 P12 Function Select
0 I/O Port
1 SEG10

P1FSR1 P11 Function Select
0 I/O Port
1 SEG9

P1FSR0 P10 Function Select
0 I/O Port
1 SEG8

8.4 P2 PORT

8.4.1 REGISTER DESCRIPTION FOR P2

P2 (P2 Data Register) : 90H

.7	.6	.5	.4	.3	.2	.1	.0
P27	P26	P25	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2[7:0] I/O Data

P2IO (P2 Direction Register) : B9H

.7	.6	.5	.4	.3	.2	.1	.0
P27IO	P26IO	P25IO	P24IO	P23IO	P22IO	P21IO	P20IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2IO[7:0] P2 Data I/O Direction

0 Input

1 Output

P2OD (P2 Open-drain Selection Register) : D4H

.7	.6	.5	.4	.3	.2	.1	.0
P27OD	P26OD	P25OD	P24OD	P23OD	P22OD	P21OD	P20OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2OD[7:0] Configure Open-drain of P2 Port

0 Push-pull output

1 Open-drain output

P2PU (P2 Pull-up Resistor Selection Register) : DCH

.7	.6	.5	.4	.3	.2	.1	.0
P27PU	P26PU	P25PU	P24PU	P23PU	P22PU	P21PU	P20PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2PU[7:0] Configure Pull-up Resistor of P2 Port

0 Disable

1 Enable

P2FSR (Port 2 Function Selection Register) : EBH

.7	.6	.5	.4	.3	.2	.1	.0
P2FSR7	P2FSR6	P2FSR5	P2FSR4	P2FSR3	P2FSR2	P2FSR1	P2FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2FSR7 P27 Function Select
0 I/O Port
1 SEG23 Function

P2FSR6 P26 Function Select
0 I/O Port
1 SEG22 Function

P2FSR5 P25 Function Select
0 I/O Port
1 SEG21 Function

P2FSR4 P24 Function Select
0 I/O Port
1 SEG20 Function

P2FSR3 P23 Function Select
0 I/O Port
1 SEG19 Function

P2FSR2 P22 Function Select
0 I/O Port
1 SEG18 Function

P2FSR1 P21 Function Select
0 I/O Port
1 SEG17 Function

P2FSR0 P20 Function Select
0 I/O Port
1 SEG16 Function

8.5 P3 PORT

8.5.1 REGISTER DESCRIPTION FOR P3

P3 (P3 Data Register) : 98H

.7	.6	.5	.4	.3	.2	.1	.0
P37	P36	P35	P34	P33	P32	P31	P30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3[7:0] I/O Data

P3IO (P3 Direction Register) : C1H

.7	.6	.5	.4	.3	.2	.1	.0
P37IO	P36IO	P35IO	P34IO	P33IO	P32IO	P31IO	P30IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3IO[7:0] P3 Data I/O Direction

0 Input (EINT0 – EINT7 function possible when input)

1 Output

P3OD (P3 Open-drain Selection Register) : D5H

.7	.6	.5	.4	.3	.2	.1	.0
P37OD	P36OD	P35OD	P34OD	P33OD	P32OD	P31OD	P30OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3OD[7:0] Configure Open-drain of P3 Port

0 Push-pull output

1 Open-drain output

P3PU (P3 Pull-up Resistor Selection Register) : DDH

.7	.6	.5	.4	.3	.2	.1	.0
P37PU	P36PU	P35PU	P34PU	P33PU	P32PU	P31PU	P30PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3PU[7:0] Configure Pull-up Resistor of P3 Port

0 Disable

1 Enable

P3DB (P3 Debounce Enable High Register) : 94H

.7	.6	.5	.4	.3	.2	.1	.0
P37DB	P36DB	P35DB	P34DB	P33DB	P32DB	P31DB	P30DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P37DB Configure Debounce of P37 Port

0 Disable

1 Enable

P36DB Configure Debounce of P36 Port

0 Disable

1 Enable

P35DB Configure Debounce of P35 Port

0 Disable

1 Enable

P34DB Configure Debounce of P34 Port

0 Disable

1 Enable

P33DB Configure Debounce of P33 Port

0 Disable

1 Enable

P32DB Configure Debounce of P32 Port

0 Disable

1 Enable

P31DB Configure Debounce of P31 Port

0 Disable

1 Enable

P30DB Configure Debounce of P30 Port

0 Disable

1 Enable

Notes:

1. If the same level is not detected on an enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clocks or more to be actually detected as a valid edge.
3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.
4. Refer to the port 4 debounce enable register (P4DB) for the debounce clock of port 3.

P3FSRH (Port 3 Function Selection High Register) : EDH

.7	.6	.5	.4	.3	.2	.1	.0
P3FSRH7	P3FSRH6	P3FSRH5	P3FSRH4	P3FSRH3	P3FSRH2	P3FSRH1	P3FSRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3FSRH[7:6] P37 Function Select

P3FSRH7	P3FSRH6	Description
0	0	I/O Port (EINT7 function possible when input)
0	1	SEG31 Function
1	0	AN7 Function
1	1	LCDBL1 Function

P3FSRH[5:4] P36 Function Select

P3FSRH5	P3FSRH4	Description
0	0	I/O Port (EINT6 function possible when input)
0	1	SEG30 Function
1	0	AN6 Function
1	1	LCDBL0 Function

P3FSRH[3:2] P35 Function Select

P3FSRH3	P3FSRH2	Description
0	0	I/O Port (EINT5 function possible when input)
0	1	SEG29 Function
1	0	VO2 Function
1	1	Not available

P3FSRH[1:0] P34 Function Select

P3FSRH1	P3FSRH0	Description
0	0	I/O Port (EINT4 function possible when input)
0	1	SEG28 Function
1	0	VI2 Function
1	1	Not available

P3FSRL (Port 3 Function Selection Low Register) : ECH

.7	.6	.5	.4	.3	.2	.1	.0
P3FSRL7	P3FSRL6	P3FSRL5	P3FSRL4	–	P3FSRL2	–	P3FSRL0
R/W	R/W	R/W	R/W	–	R/W	–	R/W

Initial value: 00H

P3FSRL[7:6] P33 Function Select

P3FSRL7	P3FSRL6	Description
0	0	I/O Port (EINT3 function possible when input)
0	1	SEG27 Function
1	0	VO1 Function
1	1	Not available

P3FSRL[5:4] P32 Function Select

P3FSRL5	P3FSRL4	Description
0	0	I/O Port (EINT2 function possible when input)
0	1	SEG26 Function
1	0	VI1 Function
1	1	Not available

P3FSRL2 P31 Function Select

0	I/O Port (EINT1 function possible when input)
1	SEG25 Function

P3FSRL0 P30 Function Select

0	I/O Port (EINT0 function possible when input)
1	SEG24 Function

8.6 P4 PORT

8.6.1 REGISTER DESCRIPTION FOR P4

P4 (P4 Data Register) : A0H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	P45	P44	P43	P42	P41	P40
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4[5:0] I/O Data

P4IO (P4 Direction Register) : C9H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	P45IO	P44IO	P43IO	P42IO	P41IO	P40IO
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4IO[5:0] P4 Data I/O Direction

0 Input (EINT12 and EINT13 function possible when input)

1 Output

P4OD (P4 Open-drain Selection Register) : D6H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	P45OD	P44OD	P43OD	P42OD	P41OD	P40OD
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4OD[5:0] Configure Open-drain of P4 Port

0 Push-pull output

1 Open-drain output

P4PU (P4 Pull-up Resistor Selection Register) : DEH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	P45PU	P44PU	P43PU	P42PU	P41PU	P40PU
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4PU[5:0] Configure Pull-up Resistor of P4 Port

0 Disable

1 Enable

P4DB (P4 Debounce Enable Register) : 95H

.7	.6	.5	.4	.3	.2	.1	.0
DBCLK1	DBCLK0	–	–	–	–	P41DB	P40DB
R/W	R/W	–	–	–	–	R/W	R/W

Initial value: 00H

DBCLK[1:0] Configure Debounce Clock of Port

DBCLK1	DBCLK0	description
0	0	fx (SCLK)
0	1	fx/4
1	0	fx/4096
1	1	fx/32

P41DB Configure Debounce of P41 Port

0	Disable
1	Enable

P40DB Configure Debounce of P40 Port

0	Disable
1	Enable

Notes:

1. If the same level is not detected on an enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clocks or more to be actually detected as a valid edge.
3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.

P4FSRH (Port 4 Function Selection High Register) : EFH

.7	.6	.5	.4	.3	.2	.1	.0
SUBMST1	SUBMST0	–	–	–	P4FSRH2	P4FSRH1	P4FSRH0
R/W	R/W	–	–	–	R/W	R/W	R/W

Initial value: 00H

SUBMST[1:0] P43 – P45 Sub Function Master Bits

SUBMST1	SUBMST0	Description
Other values		P43 - P45 functions are configured by the P4FSRHn bits (n = 0, 1, and 2)
1	0	VREG, SXIN, and SXOUT functions regardless of the P4FSRHn bits (n = 0, 1, and 2)

P4FSRH2 P45 Function Select

0	I/O Port
1	AN5 Function

P4FSRH1 P44 Function Select

0	I/O Port
1	AN4 Function

P4FSRH0 P43 Function Select

0	I/O Port
1	AN3 Function

Notes: 1. The P4FSRH register won't be changed during the f_{XIN} is selected as the system clock (fx).
2. The pull-up resistor of P44/P45 is automatically disabled regardless of P44PU/P45PU value if the P44/P45 is configured as an x-tal function (VREG/SXIN/SXOUT).

P4FSRL (Port 4 Function Selection Low Register) : EEH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	P4FSRL5	P4FSRL4	P4FSRL3	P4FSRL2	P4FSRL1	P4FSRL0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4FSRL[5:4] P42 Function Select

P4FSRL5	P4FSRL4	Description
0	0	I/O Port
0	1	EC2 Function
1	0	AN2 Function
1	1	Not available

P4FSRL[3:2] P41 Function Select

P4FSRL3	P4FSRL2	Description
0	0	I/O Port (EINT12 function possible when input)
0	1	T2O/PWM2O Function
1	0	AN1 Function
1	1	XOUT Function

P4FSRL[1:0] P40 Function Select

P4FSRL1	P4FSRL0	Description
0	0	I/O Port (EINT13 function possible when input)
0	1	T3O/PWM3O Function
1	0	AN0 Function
1	1	XIN Function

Notes: 1. Refer to the configure option for the P42/RESETB.
2. The pull-up resistor of P40/P41 is automatically disabled regardless of P40PU/P41PU value if the P40/P41 is configured as an x-tal function (XIN/XOUT).
3. The P4FSRL[3:0] bits won't be changed during the f_{XIN} is selected as the system clock (fx).

8.7 P5 PORT

8.7.1 REGISTER DESCRIPTION FOR P5

P5 (P5 Data Register) : B0H

.7	.6	.5	.4	.3	.2	.1	.0
–	P56	P55	P54	P53	P52	P51	P50
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5[6:0] I/O Data

P5IO (P5 Direction Register) : D1H

.7	.6	.5	.4	.3	.2	.1	.0
–	P56IO	P55IO	P54IO	P53IO	P52IO	P51IO	P50IO
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5IO[6:0] P5 Data I/O Direction

0 Input

1 Output

P5OD (P5 Open-drain Selection Register) : D7H

.7	.6	.5	.4	.3	.2	.1	.0
–	P56OD	P55OD	P54OD	P53OD	P52OD	P51OD	P50OD
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5OD[6:0] Configure Open-drain of P5 Port

0 Push-pull output

1 Open-drain output

P5PU (P5 Pull-up Resistor Selection Register) : DFH

.7	.6	.5	.4	.3	.2	.1	.0
–	P56PU	P55PU	P54PU	P53PU	P52PU	P51PU	P50PU
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5PU[6:0] Configure Pull-up Resistor of P5 Port

0 Disable

1 Enable

P5FSR (Port 5 Function Selection Register) : F1H

.7	.6	.5	.4	.3	.2	.1	.0
–	P5FSR6	P5FSR5	P5FSR4	P5FSR3	P5FSR2	P5FSR1	P5FSR0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5FSR6 P56 Function Select
- 0 I/O Port
- 1 COM1 Function

P5FSR5 P55 Function Select
- 0 I/O Port
- 1 COM0 Function

P5FSR4 P54 Function Select
- 0 I/O Port
- 1 CAPL Function

P5FSR3 P53 Function Select
- 0 I/O Port
- 1 CAPH Function

P5FSR2 P52 Function Select
- 0 I/O Port
- 1 VLC3 Function

P5FSR1 P51 Function Select
- 0 I/O Port
- 1 VLC2 Function

P5FSR0 P50 Function Select
- 0 I/O Port
- 1 VLC0 Function

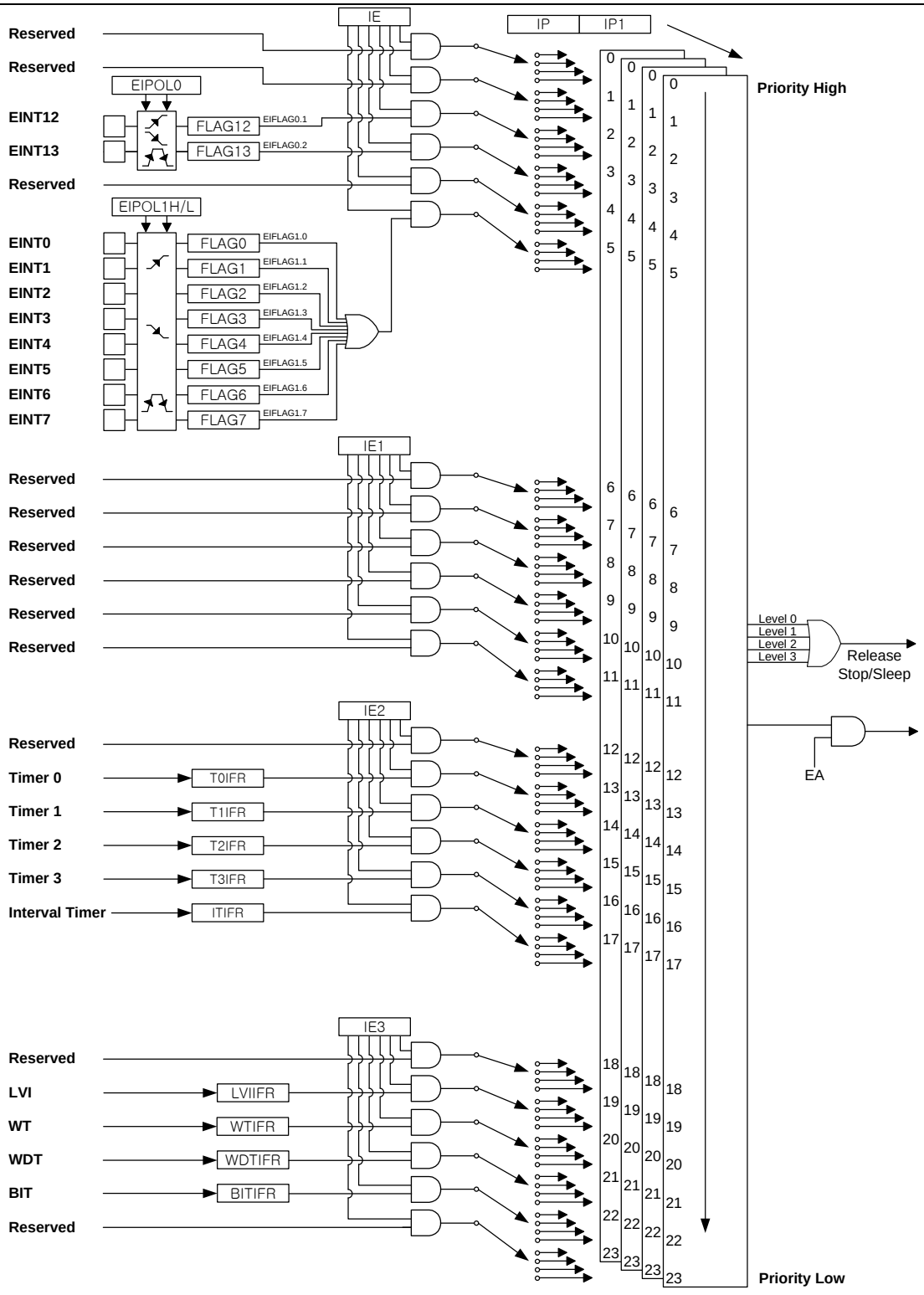
9. INTERRUPT CONTROLLER

9.1 INTERRUPT GROUP PRIORITY LEVEL

Interrupt Group	Highest → Lowest				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	Lowest

Interrupt Group Priority Level

9.2 INTERRUPT BLOCK DIAGRAM



Notes: 1. The release signal may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

9.3 INTERRUPT VECTOR TABLE

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware RESET	RESETB	0 0	0	Non-Maskable	0000H
–	INT0	IE.0	1	Maskable	0003H
–	INT1	IE.1	2	Maskable	000BH
External Interrupt 12	INT2	IE.2	3	Maskable	0013H
External Interrupt 13	INT3	IE.3	4	Maskable	001BH
–	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 – 7	INT5	IE.5	6	Maskable	002BH
–	INT6	IE1.0	7	Maskable	0033H
–	INT7	IE1.1	8	Maskable	003BH
–	INT8	IE1.2	9	Maskable	0043H
–	INT9	IE1.3	10	Maskable	004BH
–	INT10	IE1.4	11	Maskable	0053H
–	INT11	IE1.5	12	Maskable	005BH
–	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
Interval Timer Match Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
LVI Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
–	INT23	IE3.5	24	Maskable	00BBH

9.3.1 REGISTER MAP

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Priority Register
IP1	F8H	R/W	00H	Interrupt Priority Register 1
EIFLAG0	A3H	R/W	00H	External Interrupt Flag 0 Register
EIPOL0	A4H	R/W	00H	External Interrupt Polarity 0 Register
EIFLAG1	A5H	R/W	00H	External Interrupt Flag 1 Register
EIPOL1L	A6H	R/W	00H	External Interrupt Polarity 1 Low Register
EIPOL1H	A7H	R/W	00H	External Interrupt Polarity 1 High Register

Register Map

9.3.2 REGISTER DESCRIPTION FOR INTERRUPT

IE (Interrupt Enable Register) : A8H

.7	.6	.5	.4	.3	.2	.1	.0
EA	–	INT5E	–	INT3E	INT2E	–	–
R/W	–	R/W	–	R/W	R/W	–	–

Initial value: 00H

EA Enable or disable all interrupt bits

0 All interrupt disable

1 All interrupt enable

INT5E Enable or disable External interrupt 0 – 7 (EINT0 – EINT7)

0 Disable

1 Enable

INT3E Enable or disable External interrupt 13 (EINT13)

0 Disable

1 Enable

INT2E Enable or disable External interrupt 12 (EINT12)

0 Disable

1 Enable

IE1 (Interrupt Enable Register 1) : A9H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–

Initial value: 00H

IE2 (Interrupt Enable Register 2) : AAH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	INT17E	INT16E	INT15E	INT14E	INT13E	–
–	–	R/W	R/W	R/W	R/W	R/W	–

Initial value: 00H

INT17E Enable or disable Interval Timer match interrupt

0 Disable

1 Enable

INT16E Enable or disable Timer 3 match interrupt

0 Disable

1 Enable

INT15E Enable or disable Timer 2 match interrupt

0 Disable

1 Enable

INT14E Enable or disable Timer 1 match interrupt

0 Disable

1 Enable

INT13E Enable or disable Timer 0 match interrupt

0 Disable

1 Enable

IE3 (Interrupt Enable Register 3) : ABH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	INT22E	INT21E	INT20E	INT19E	INT18E
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

INT22E Enable or disable BIT interrupt
0 Disable
1 Enable

INT21E Enable or disable WDT interrupt
0 Disable
1 Enable

INT20E Enable or disable WT interrupt
0 Disable
1 Enable

INT19E Enable or disable LVI interrupt
0 Disable
1 Enable

INT18E Enable or disable ADC interrupt
0 Disable
1 Enable

IP (Interrupt Priority Register) : B8H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	IP5	IP4	IP3	IP2	IP1	IP0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IP1 (Interrupt Priority Register 1) : F8H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	IP15	IP14	IP13	IP12	IP11	IP10
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IP[5:0], IP1[5:0] Select Interrupt Group Priority

IP1x	IPx	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIFLAG0 (External Interrupt Flag 0 Register) : A3H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	FLAG13	FLAG12	–
–	–	–	–	–	R/W	R/W	–

Initial value: 00H

FLAG13 When an external interrupt 13 is occurred, the flag becomes '1'. The flag is cleared by writing '0' to the bit or automatically cleared by INT_ACK signal.

0 External Interrupt not occurred

1 External Interrupt occurred

FLAG12 When an external interrupt 12 is occurred, the flag becomes '1'. The flag is cleared by writing '0' to the bit or automatically cleared by INT_ACK signal.

0 External Interrupt not occurred

1 External Interrupt occurred

EIPOL0 (External Interrupt Polarity 0 Register) : A4H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	POL13		POL12		–	–
–	–	R/W	R/W	R/W	R/W	–	–

Initial value: 00H

EIPOL0[7:0] External interrupt (EINT12, EINT13) polarity selection

POLn[1:0]		Description
0	0	No interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 12 and 13

EIFLAG1 (External Interrupt Flag 1 Register) : A5H

.7	.6	.5	.4	.3	.2	.1	.0
FLAG7	FLAG6	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	FLAG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

EIFLAG1[7:0] When an external interrupt is occurred, the flag becomes '1'. The flag is cleared only by writing '0' to the bit. So, the flag should be cleared by software.

0 External Interrupt not occurred

1 External Interrupt occurred

EIPOL1H (External Interrupt Polarity 1 High Register) : A7H

.7	.6	.5	.4	.3	.2	.1	.0
POL7		POL6		POL5		POL4	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

EIPOL1H[7:0] External interrupt (EINT4,,,,,,, EINT7) polarity selection

POLn[1:0]		Description
0	0	No interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 4, 5, 6, and 7

EIPOL1L (External Interrupt Polarity 1 Low Register) : A6H

.7	.6	.5	.4	.3	.2	.1	.0
POL3		POL2		POL1		POL0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

EIPOL1L[7:0] External interrupt (EINT0,,,,,,, EINT3) polarity selection

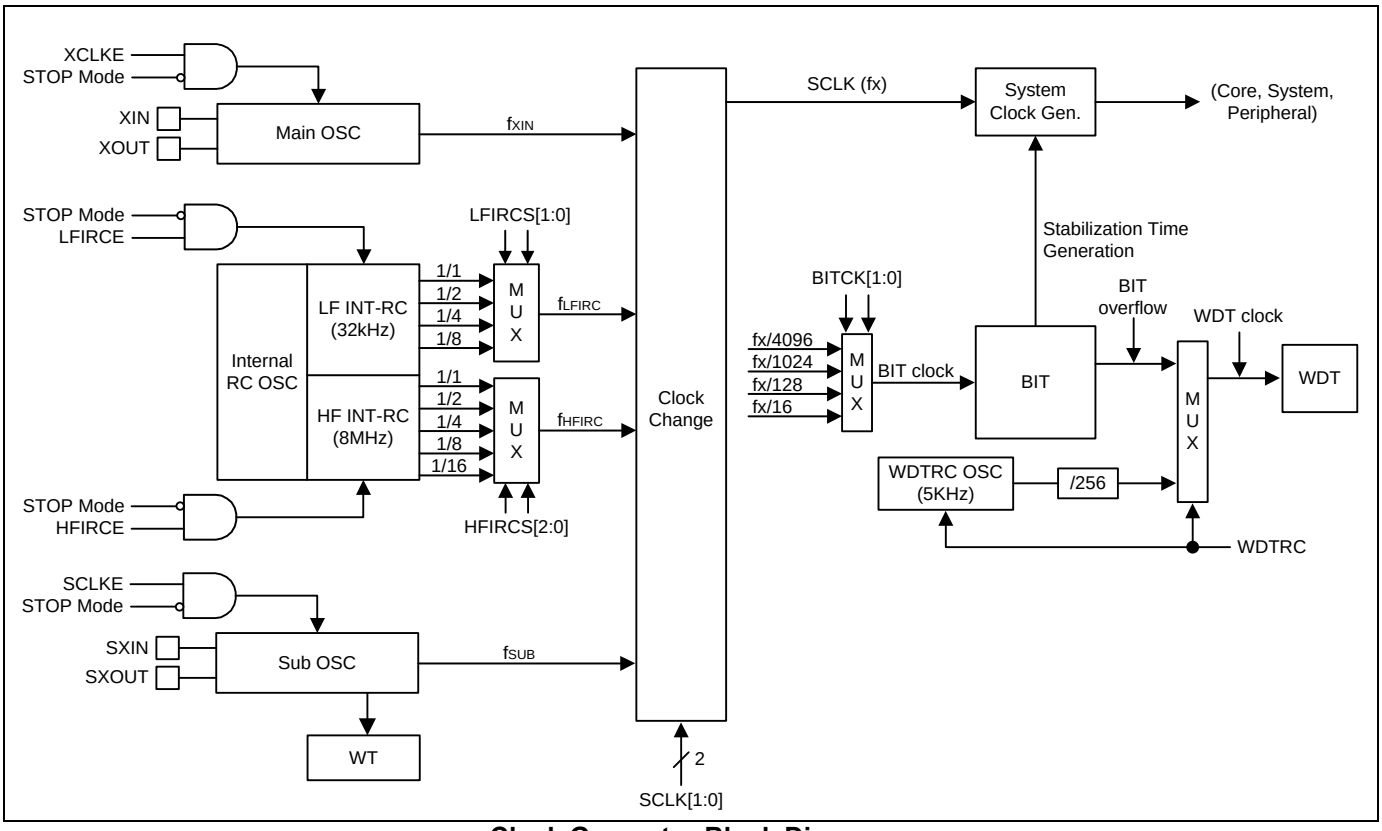
POLn[1:0]		Description
0	0	No interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 0, 1, 2, and 3

10. PERIPHERAL HARDWARE

10.1 CLOCK GENERATOR

10.1.1 BLOCK DIAGRAM



Clock Generator Block Diagram

10.1.2 REGISTER MAP

Name	Address	Dir	Default	Description
SCCR	8AH	R/W	00H	System and Clock Control Register
OSCCR	C8H	R/W	08H	Oscillator Control Register
LIFSR	BFH	R/W	00H	LFIRC Frequency Selection Register
IRCTCR	8FH	R/W	00H	Internal RC Trim Control Register
IRCTRM	97H	R/W	xxH	Internal RC Trim Register
IRCIDR	E7H	R/W	00H	Internal RC Identification Register

Register Map

10.1.3 REGISTER DESCRIPTION CLOCK GENERATOR

SCCR (System and Clock Control Register) : 8AH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	–	SCLK1	SCLK0
–	–	–	–	–	–	R/W	R/W

Initial value: 00H

SCLK[1:0] System Clock Selection Bit

SCLK1	SCLK0	Description
0	0	HF INT-RC OSC (f_{HFIRC}) for system clock
0	1	External Main OSC (f_{XIN}) for system clock
1	0	External Sub OSC (f_{SUB}) for system clock
1	1	LF INT-RC OSC (f_{LFIRC}) for system clock

Note: If a target system clock is disabled by the OSCCR register, the SCCR register won't be changed in case of selecting the corresponding clock as a system clock.

OSCCR (Oscillator Control Register) : C8H

.7	.6	.5	.4	.3	.2	.1	.0
LFIRCE	–	HFIRCS2	HFIRCS1	HFIRCS0	HFIRCE	XCLKE	SCLKE
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 08H

LFIRCE Control the operation of the low frequency internal RC oscillator

0 Disable operation of LFIRC OSC

1 Enable operation of LFIRC OSC

HFIRCS[2:0] HFIRC oscillator post-divider selection

HFIRCS2	HFIRCS1	HFIRCS0	Description
0	0	0	f_{HFIRC}/16 (0.5MHz)
0	0	1	f_{HFIRC}/8 (1MHz)
0	1	0	f_{HFIRC}/4 (2MHz)
0	1	1	f_{HFIRC}/2 (4MHz)
1	0	0	f_{HFIRC}/1 (8MHz)
Other values			Not used

HFIRCE Control the operation of the high frequency internal RC oscillator

0 Enable operation of HFIRC OSC

1 Disable operation of HFIRC OSC

XCLKE Control the operation of the external main oscillator

0 Disable operation of X-TAL

1 Enable operation of X-TAL

SCLKE Control the operation of the external sub oscillator

0 Disable operation of SX-TAL

1 Enable operation of SX-TAL

Note: The system clock is not disabled by the corresponding bit of the OSCCR register.
Ex) The high frequency internal RC oscillator won't be disabled by the HFIRCE bit during the f_{HFIRC} is selected as the system clock.

LIFSR (LFIRC Frequency Selection Register) : BFH

.7	.6	.5	.4	.3	.2	.1	.0
LIWTP4	LIWTP3	LIWTP2	LIWTP1	LIWTP0	–	LFIRCS1	LFIRCS0
W	W	W	W	W	–	R/W	R/W

Initial value: 00H

LIWTP[4:0] Write Identification bits. These bits are automatically cleared to "00000b" immediately after LIFSR write. 0x00 on read.

10110b Write 0x16 to these bits with valid LFIRCS[1:0]

Other values Write is ignored.

LFIRCS [1:0] LFIRC oscillator post-divider selection.

LFIRCS1	LFIRCS0	Description
0	0	f_{LFIRC}/8 (4kHz)
0	1	f_{LFIRC}/4 (8kHz)
1	0	f_{LFIRC}/2 (16kHz)
1	1	f_{LFIRC}/1 (32kHz)

IRCIDR (Internal RC Trim Identification Register) : E7H

.7	.6	.5	.4	.3	.2	.1	.0
IRCID7	IRCID6	IRCID5	IRCID4	IRCID3	IRCID2	IRCID1	IRCID0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IRCID[7:0] Internal RC Trim Identification

Others No identification value

01000110 Identification value for IRC Trim
(These bits are automatically cleared to logic '00H' immediately after one time operation)

IRCTRM (Internal RC Trim Register) : 97H

.7	.6	.5	.4	.3	.2	.1	.0
ITRM7	ITRM6	ITRM5	ITRM4	ITRM3	ITRM2	ITRM1	ITRM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: xxH

ITRM[7:0] Internal RC Trim bits

These bits are read from "Configure Area" when a system reset occurs. These bits provide a user programmable trimming value on operation. The range is -128 to +127. The ITRM7 is sign bit. The IRC frequency is faster by minus value and slower by plus. The frequency is changed by 2.5[kHz] step-by-step. This register can be written with valid ID value and IRCTCR=0xB3.

IRCTCR (Internal RC Trim Control Register) : 8FH

.7	.6	.5	.4	.3	.2	.1	.0
ITCR7	ITCR6	ITCR5	ITCR4	ITCR3	ITCR2	ITCR1	ITCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

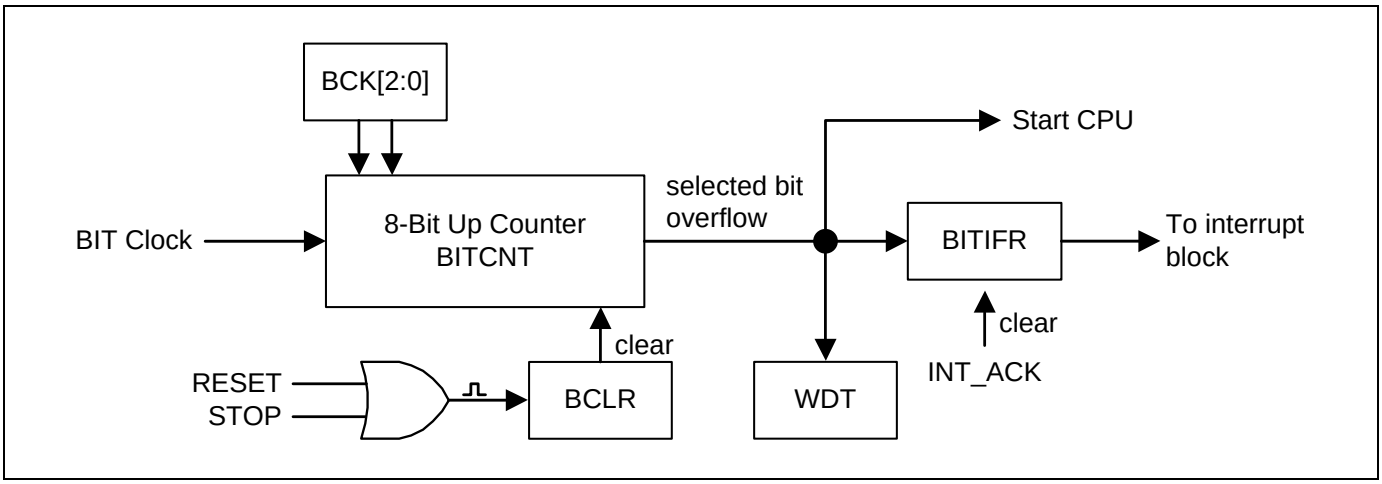
ITCR[7:0] Internal RC Trim Control Register

Others No effect

10110011 IRCTRM register is used for IRC frequency.
This register can be written with valid ID value.

10.2 BIT

10.2.1 BLOCK DIAGRAM



BIT Block Diagram

10.2.2 REGISTER MAP

Name	Address	Dir	Default	Description
BITCR	8BH	R/W	01H	Basic Interval Timer Control Register
BITCNT	8CH	R	00H	Basic Interval Timer Counter Register

Register Map

10.2.3 REGISTER DESCRIPTION FOR BASIC INTERVAL TIMER

BITCNT (Basic Interval Timer Counter Register) : 8CH

.7	.6	.5	.4	.3	.2	.1	.0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R	R	R	R	R	R	R	R

Initial value: 00H

BIT[7:0] BIT Counter

BITCR (Basic Interval Timer Control Register) : 8BH

.7	.6	.5	.4	.3	.2	.1	.0
BITIFR	BITCK1	BITCK0	–	BCLR	BCK2	BCK1	BCK0
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

Initial value: 01H

BITIFR When BIT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 BIT Interrupt no generation
1 BIT Interrupt generation

BITCK[1:0] Select BIT Clock Source

BITCK1	BITCK0	description
0	0	fx/4096
0	1	fx/1024
1	0	fx/128
1	1	fx/16

BCLR If this bit is written to '1', BIT counter is cleared as '0'

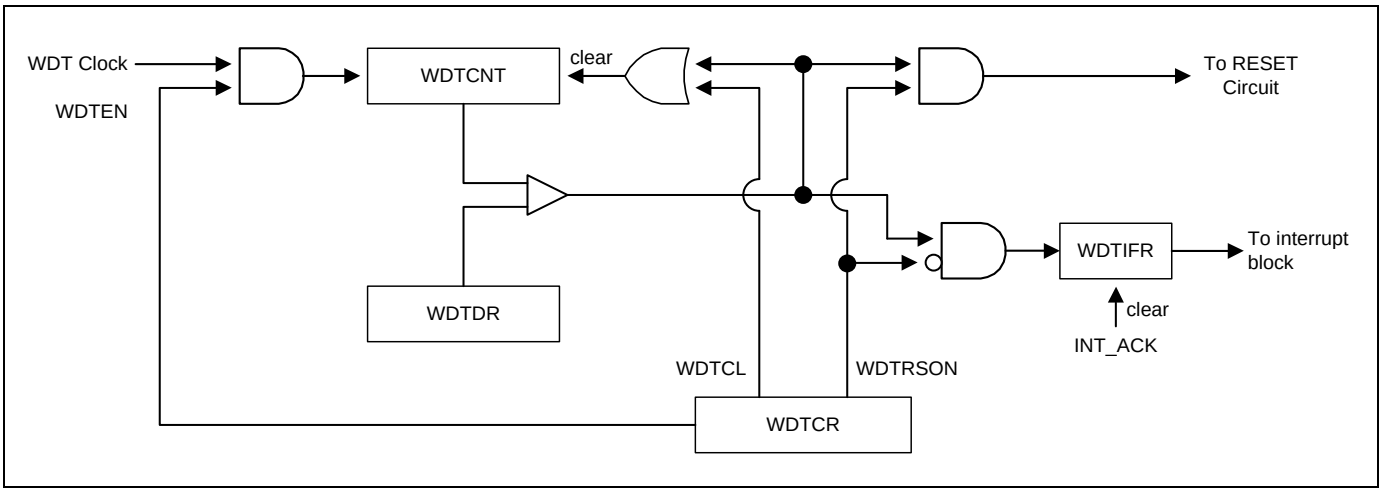
0 Free running
1 Clear counter

BCK[2:0] Select BIT overflow period

BCK2	BCK1	BCK0	description
0	0	0	Bit 0 overflow (BIT Clock *2)
0	0	1	Bit 1 overflow (BIT Clock *4) (default)
0	1	0	Bit 2 overflow (BIT Clock *8)
0	1	1	Bit 3 overflow (BIT Clock *16)
1	0	0	Bit 4 overflow (BIT Clock *32)
1	0	1	Bit 5 overflow (BIT Clock *64)
1	1	0	Bit 6 overflow (BIT Clock *128)
1	1	1	Bit 7 overflow (BIT Clock *256)

10.3 WDT

10.3.1 BLOCK DIAGRAM



WDT Block Diagram

10.3.2 REGISTER MAP

Name	Address	Dir	Default	Description
WDTDR	8EH	W	FFH	Watch Dog Register
WDTCNT	8EH	R	00H	Watch Dog Timer Counter Register
WDTCR	8DH	R/W	00H	Watch Dog Timer Control Register

Register Map

10.3.3 REGISTER DESCRIPTION FOR WATCH DOG TIMER

WDTCNT (Watch Dog Timer Counter Register : Read Case) : 8EH

.7	.6	.5	.4	.3	.2	.1	.0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value: 00H

WDTCNT[7:0] WDT Counter

WDTDR (Watch Dog Timer Data Register : Write Case) : 8EH

.7	.6	.5	.4	.3	.2	.1	.0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value: FFH

WDTDR[7:0] Set a period

WDT Interrupt Interval=(BIT Interval)X(WDTDR Value +1)

Note: Do not write ‘0’ in the WDTDR register.

WDTCR (Watch Dog Timer Control Register) : 8DH

.7	.6	.5	.4	.3	.2	.1	.0
WDTEN	WDTRSON	WDTCL	–	–	–	WDTCK	WDTIFR
R/W	R/W	R/W	–	–	–	R/W	R/W

Initial value: 00H

WDTEN Control WDT operation

0 Disable

1 Enable

WDTRSON Control WDT RESET operation

0 Free running 8-bit timer

1 Watch Dog Timer RESET ON

WDTCL Clear WDT Counter

0 Free run

1 Clear WDT Counter (auto clear after 1 cycle)

WDTCK Control WDT Clock Selection Bit

0 BIT overflow for WDT clock (WDTRC disable)

1 WDTRC for WDT clock (WDTRC Enable)

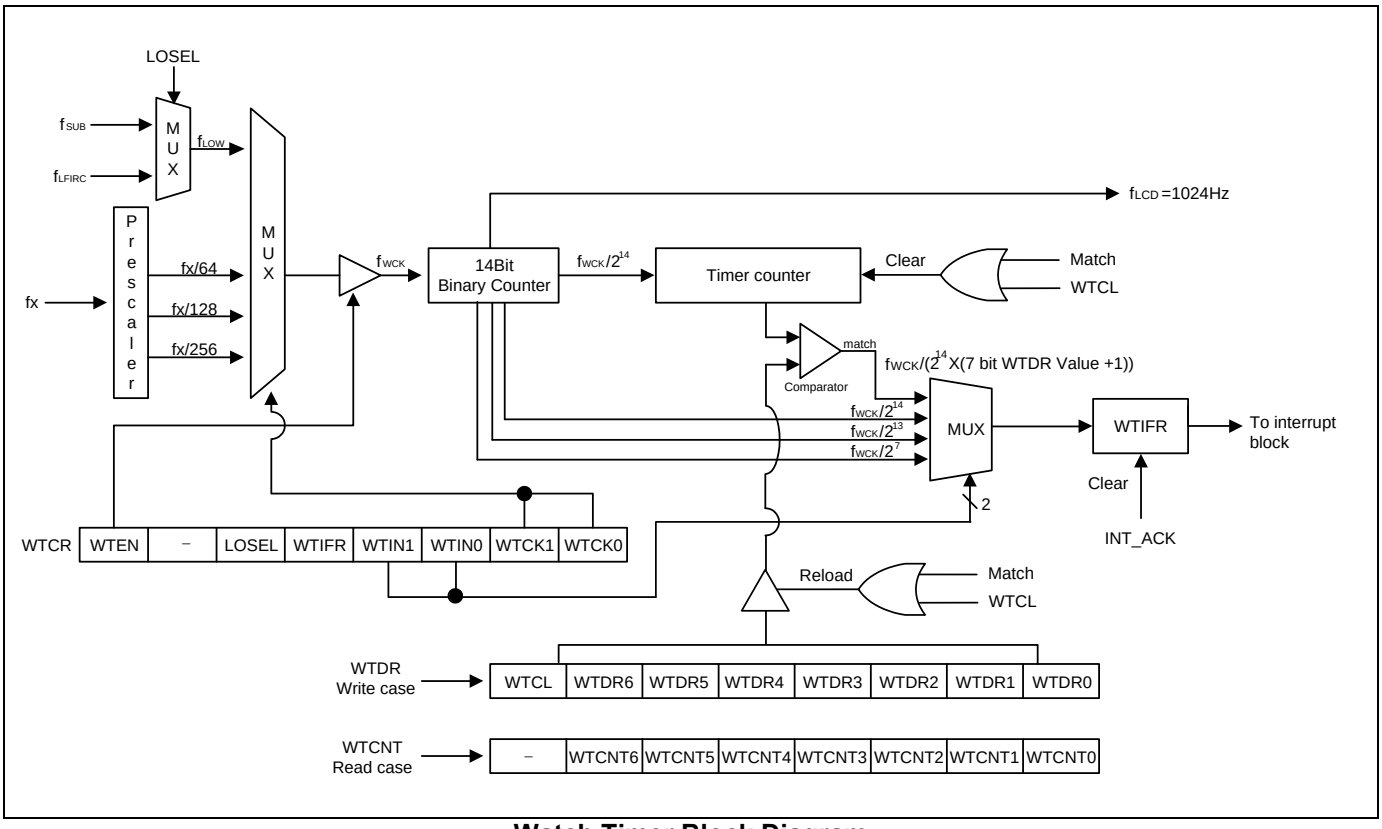
WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 WDT Interrupt no generation

1 WDT Interrupt generation

10.4 WT

10.4.1 BLOCK DIAGRAM



Watch Timer Block Diagram

10.4.2 REGISTER MAP

Name	Address	Dir	Default	Description
WTCR	96H	R/W	00H	Watch Timer Control Register
WTDR	89H	W	7FH	Watch Timer Data Register
WTCNT	89H	R	00H	Watch Timer Counter Register

Register Map

10.4.3 REGISTER DESCRIPTION FOR WATCH TIMER

WTCNT (Watch Timer Counter Register : Read Case) : 89H

.7	.6	.5	.4	.3	.2	.1	.0
–	WTCNT6	WTCNT5	WTCNT4	WTCNT3	WTCNT2	WTCNT1	WTCNT0
–	R	R	R	R	R	R	R

Initial value: 00H

WTCNT[6:0] WT Counter

WTDR (Watch Timer Register : Write Case) : 89H

.7	.6	.5	.4	.3	.2	.1	.0
WTCL	WTDR6	WTDR5	WTDR4	WTDR3	WTDR2	WTDR1	WTDR0
R/W	W	W	W	W	W	W	W

Initial value: 7FH

WTCL Clear WT Counter

0 Free Run

1 Clear WT Counter (auto clear after 1 cycle)

WTDR[6:0] Set WT period

WT Interrupt interval = fwck/(2^14 X (7bit WTDR Value +1))

Note: Do not write ‘0’ in the WTDR register.

WTCR (Watch Timer Control Register) : 96H

.7	.6	.5	.4	.3	.2	.1	.0
WTEN	–	LOSEL	WTIFR	WTIN1	WTIN0	WTCK1	WTCK0
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

WTEN Control Watch Timer

0 Disable

1 Enable

LOSEL Select Low Frequency

0 fsub

1 f_{LFIRC}

WTIFR When WT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 WT Interrupt no generation

1 WT Interrupt generation

WTIN[1:0] Determine interrupt interval

WTIN1	WTIN0	description
0	0	fwck/2^7
0	1	fwck/2^13
1	0	fwck/2^14
1	1	fwck/(2^14 X (7bit WTDR Value + 1))

WTCK[1:0] Determine source clock

WTCK1	WTCK0	description
0	0	f_{LOW}
0	1	fx/256
1	0	fx/128
1	1	fx/64

Note: fx –System clock frequency (where fx=4.19MHz)

fsub – Sub clock oscillator frequency (32.768kHz)

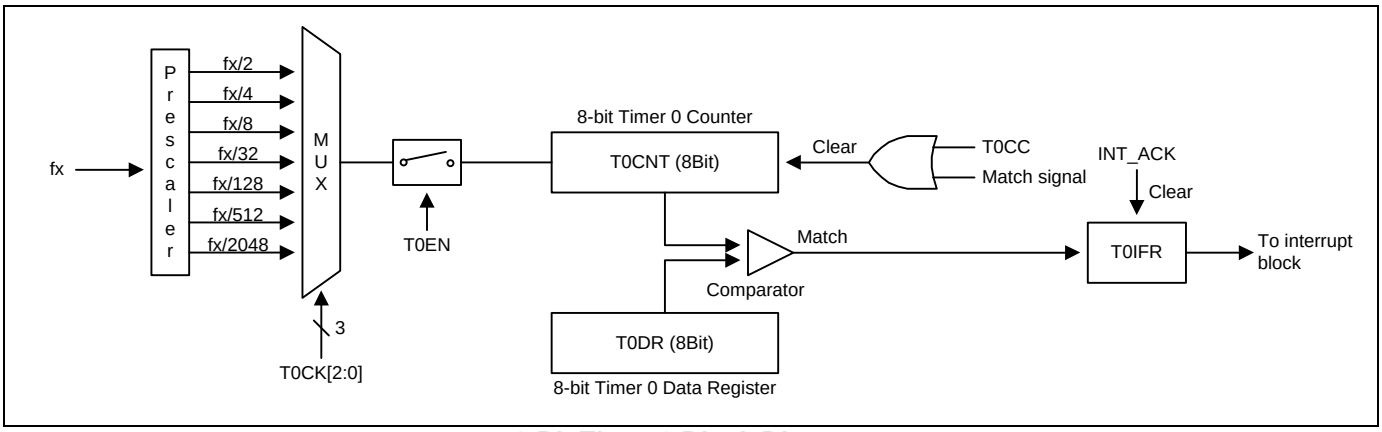
f_{LFIRC} – Low frequency IRC (32kHz)

fwck – Select Watch Timer clock

f_{LCD} – LCD frequency (where fx=4.19MHz, WTCK[1:0]='10'; f_{LCD} = 1024Hz)

10.5 TIMER0

10.5.1 BLOCK DIAGRAM



8-Bit Timer 0 Block Diagram

10.5.2 REGISTER MAP

Name	Address	Dir	Default	Description
T0CR	B2H	R/W	00H	Timer 0 Control Register
T0CNT	B3H	R	00H	Timer 0 Counter Register
T0DR	B4H	R/W	FFH	Timer 0 Data Register

Register Map

10.5.3 REGISTER DESCRIPTION FOR TIMER 0

T0CNT (Timer 0 Counter Register) : B3H

.7	.6	.5	.4	.3	.2	.1	.0
T0CNT7	T0CNT6	T0CNT5	T0CNT4	T0CNT3	T0CNT2	T0CNT1	T0CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T0CNT[7:0] T0 Counter

T0DR (Timer 0 Data Register) : B4H

.7	.6	.5	.4	.3	.2	.1	.0
T0DR7	T0DR6	T0DR5	T0DR4	T0DR3	T0DR2	T0DR1	T0DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T0DR[7:0] T0 Data

T0CR (Timer 0 Control Register) : B2H

.7	.6	.5	.4	.3	.2	.1	.0
T0EN	T0IFR	–	–	T0CK2	T0CK1	T0CK0	T0CC
R/W	R/W	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

T0EN Control Timer 0

0 Timer 0 disable

1 Timer 0 enable

T0IFR When T0 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T0 Interrupt no generation

1 T0 Interrupt generation

T0CK[2:0] Select Timer 0 clock source. fx is main system clock frequency

T0CK2	T0CK1	T0CK0	description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/32
1	0	0	fx/128
1	0	1	fx/512
1	1	0	fx/2048
1	1	1	Not available

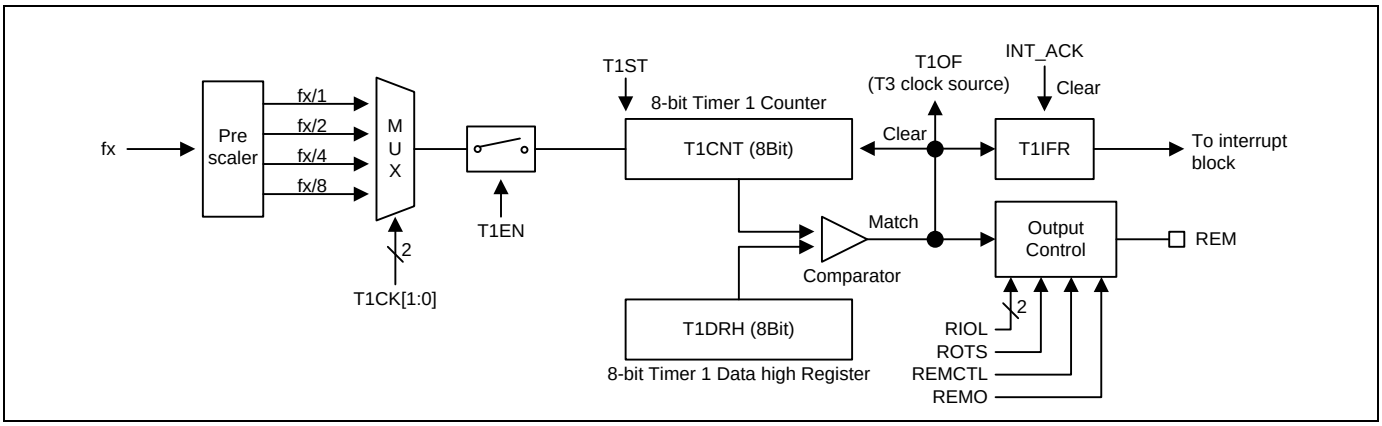
T0CC Clear Timer 0 Counter

0 No effect

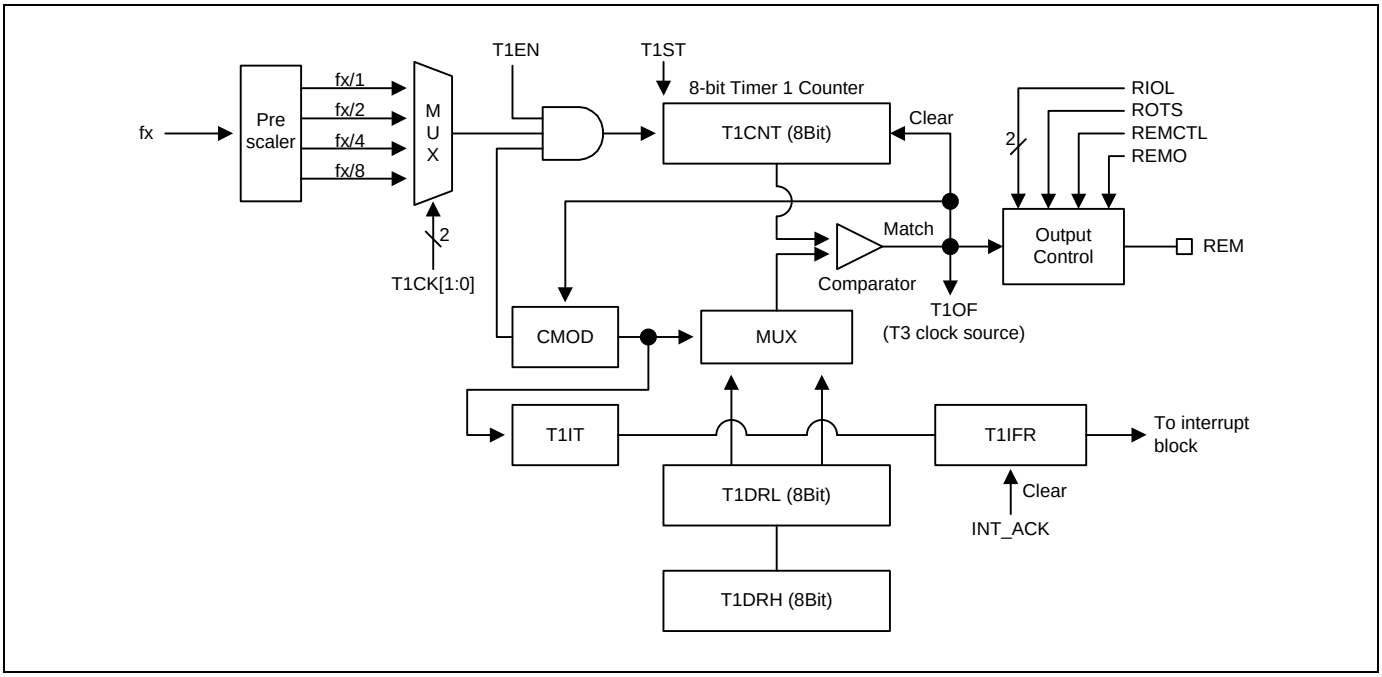
1 Clear the Timer 0 counter (When write, automatically cleared “0” after being cleared counter)

10.6 TIMER 1

10.6.1 BLOCK DIAGRAM



8-Bit Timer Counter 1 Block Diagram



Carrier Mode for Timer 1

10.6.2 REGISTER MAP

Name	Address	Dir	Default	Description
T1CR	BAH	R/W	00H	Timer 1 Control Register
CARCR	BEH	R/W	00H	Carrier control Register
T1CNT	BBH	R	00H	Timer 1 Counter Register
T1DRH	BDH	R/W	FFH	Timer 1 Data High Register
T1DRL	BCH	R/W	FFH	Timer 1 Data Low Register

Register Map

10.6.3 REGISTER DESCRIPTION FOR TIMER 1

T1CNT (Timer 1 Counter Register) : BBH

.7	.6	.5	.4	.3	.2	.1	.0
T1CNT7	T1CNT6	T1CNT5	T1CNT4	T1CNT3	T1CNT2	T1CNT1	T1CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T1CNT[7:0] T1 Counter

T1DRH (Timer 1 Data High Register) : BDH

.7	.6	.5	.4	.3	.2	.1	.0
T1DRH7	T1DRH6	T1DRH5	T1DRH4	T1DRH3	T1DRH2	T1DRH1	T1DRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T1DRH[7:0] T1 High Data

T1DRL (Timer 1 Data Low Register : Carrier mode only) : BCH

.7	.6	.5	.4	.3	.2	.1	.0
T1DRL7	T1DRL6	T1DRL5	T1DRL4	T1DRL3	T1DRL2	T1DRL1	T1DRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T1DRL[7:0] T1 Low Data

T1CR (Timer 1 Control Register) : BAH

.7	.6	.5	.4	.3	.2	.1	.0
T1EN	T1IFR	–	CAR1	T1CK1	T1CK0	T1CN	T1ST
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T1EN Control Timer 1

0 Timer 1 disable

1 Timer 1 enable

T1IFR When T1 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T1 Interrupt no generation

1 T1 Interrupt generation

CAR1 Control Timer 1 operation mode

0 Timer/counter mode

1 Carrier mode

T1CK[1:0] Select Timer 1 clock source. fx is main system clock frequency

T1CK1	T1CK0	description
0	0	fx/1
0	1	fx/2
1	0	fx/4
1	1	fx/8

T1CN Control Timer 1 Counter pause/continue

0 Temporary count stop

1 Continue count

T1ST Control Timer 1 start/stop

0 Counter stop

1 Clear counter and start

CARCR (Carrier Control Register : Carrier mode only) : BEH

.7	.6	.5	.4	.3	.2	.1	.0
RIOL1	RIOL0	T1IT1	T1IT0	ROTS	REMCTL	CMOD	REMO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

RIOL[1:0] REM Output Low Current (IOL) Capability Selection only when the ROTS bit is “0b”. The basic IOL is typical 630mA when VDD = 3V and VOL = 1.0V.

RIOL1	RIOL0	description
0	0	IOL x 0.60
0	1	IOL x 0.75
1	0	IOL x 0.90
1	1	IOL x 1.0

T1IT[1:0] T1 Interrupt time select

T1IT1	T1IT0	description
0	0	Elapsed time for low data value
0	1	Elapsed time for high data value
1	0	Elapsed time for low and high data values
1	1	Not available

ROTS REM Output Type Selection

0	N-channel open-drain output (High sink current)
1	Push-pull output (Normal CMOS)

REMCTL REM Operation Control

0	When the ROTS bit is 0, REM is high-impedance When the ROTS bit is 1, REM is high-impedance at REMO=1 and low level at REMO=0.
1	REM signal is output

CMOD Carrier Frequency Mode Select

0	One-shot mode
1	Repeating mode

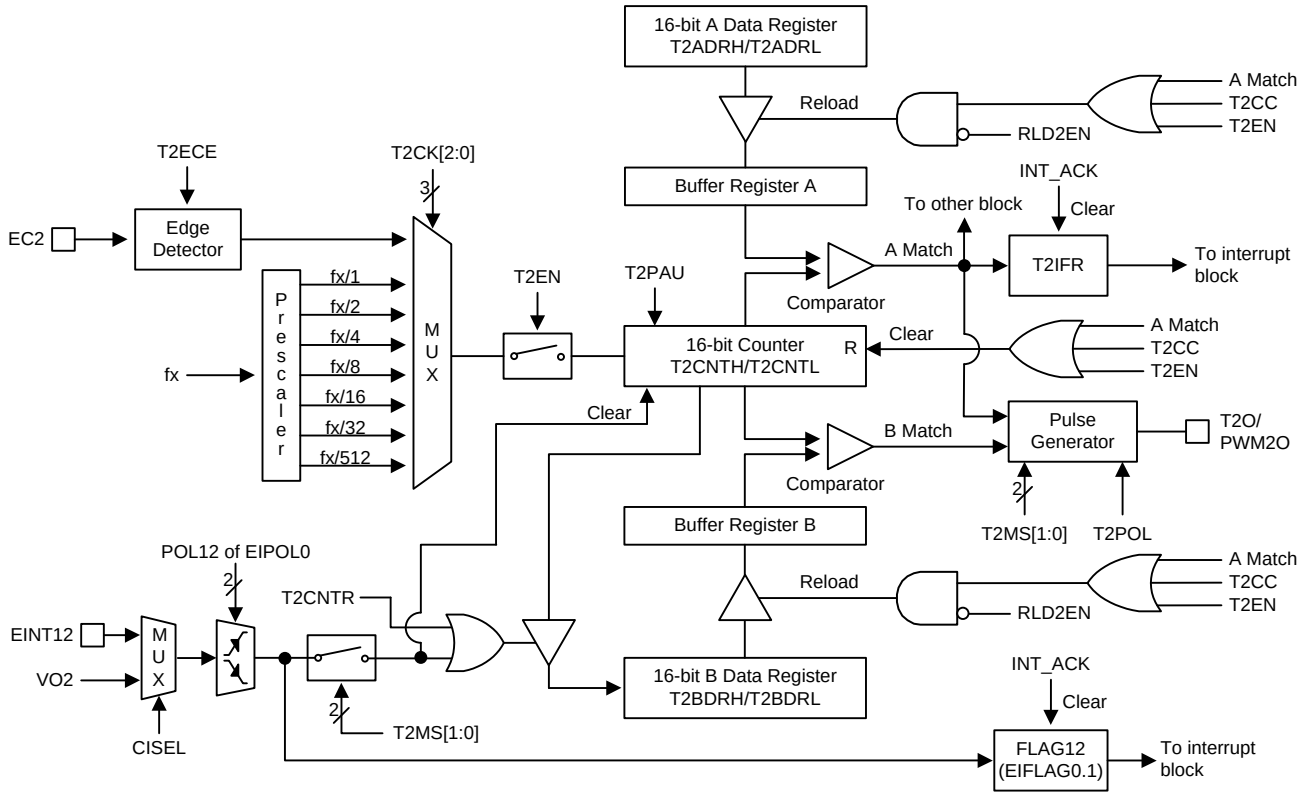
REMO REM Output Control. Where Hi-Z is high-impedance

0	T1DRL/T1DRH -> Hi-Z/Low width during ROTS=0 T1DRL/T1DRH -> Low/High width during ROTS=1
1	T1DRL/T1DRH -> Low/Hi-Z width during ROTS=0 T1DRL/T1DRH -> High/Low width during ROTS=1

Note: A VDD voltage must be less than 3.6V if the N-channel open-drain is selected for REM output type (ROTS=0).

10.7 TIMER 2

10.7.1 BLOCK DIAGRAM



Notes: 1. The T2EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. The RLD2EN bit should be “0b” when the T2EN bit is changed “0b” to “1b”.

16-Bit Timer Counter 2 Block Diagram

10.7.2 REGISTER MAP

Name	Address	Dir	Default	Description
T2CRH	C3H	R/W	00H	Timer 2 Control High Register
T2CRL	C2H	R/W	00H	Timer 2 Control Low Register
T2ADRH	C5H	R/W	FFH	Timer 2 A Data High Register
T2ADRL	C4H	R/W	FFH	Timer 2 A Data Low Register
T2BDRH	C7H	R/W	FFH	Timer 2 B Data High Register
T2BDRL	C6H	R/W	FFH	Timer 2 B Data Low Register

Register Map

10.7.3 REGISTER DESCRIPTION FOR TIMER 2

T2ADRH (Timer 2 A Data High Register) : C5H

.7	.6	.5	.4	.3	.2	.1	.0
T2ADRH7	T2ADRH6	T2ADRH5	T2ADRH4	T2ADRH3	T2ADRH2	T2ADRH1	T2ADRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T2ADRH[7:0] T2 A Data High Byte

T2ADRL (Timer 2 A Data Low Register) : C4H

.7	.6	.5	.4	.3	.2	.1	.0
T2ADRL7	T2ADRL6	T2ADRL5	T2ADRL4	T2ADRL3	T2ADRL2	T2ADRL1	T2ADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T2ADRL[7:0] T2 A Data Low Byte

T2BDRH (Timer 2 B Data High Register) : C7H

.7	.6	.5	.4	.3	.2	.1	.0
T2BDRH7	T2BDRH6	T2BDRH5	T2BDRH4	T2BDRH3	T2BDRH2	T2BDRH1	T2BDRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T2BDRH[7:0] T2 B Data High Byte

T2BDRL (Timer 2 B Data Low Register) : C6H

.7	.6	.5	.4	.3	.2	.1	.0
T2BDRL7	T2BDRL6	T2BDRL5	T2BDRL4	T2BDRL3	T2BDRL2	T2BDRL1	T2BDRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T2BDRL[7:0] T2 B Data Low Byte

T2CRH (Timer 2 Control High Register) : C3H

.7	.6	.5	.4	.3	.2	.1	.0
T2EN	–	T2MS1	T2MS0	CISEL	–	T2PAU	T2CC
R/W	–	R/W	R/W	R/W	–	R/W	R/W

Initial value: 00H

T2EN Control Timer 2

0 Timer 2 disable

1 Timer 2 enable (Counter clear and start)

T2MS[1:0] Control Timer 2 Operation Mode

T2MS1	T2MS0	description
0	0	Timer/counter mode (T2O: toggle at A match)
0	1	Capture mode (The A match interrupt can occur)
1	0	PPG one-shot mode (PWM2O)
1	1	PPG repeat mode (PWM2O)

CISEL Select Capture Input

0 EINT12

1 VO2

T2PAU Timer 2 Counter Temporary Pause Control

0 Continue counting

1 Temporary pause

T2CC Clear Timer 2 Counter

0 No effect

1 Clear the Timer 2 counter (When write, automatically cleared “0” after being cleared counter)

T2CRL (Timer 2 Control Low Register) : C2H

.7	.6	.5	.4	.3	.2	.1	.0
T2CK2	T2CK1	T2CK0	T2IFR	RLD2EN	T2POL	T2ECE	T2CNTR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T2CK[2:0] Select Timer 2 clock source. fx is system clock frequency

T2CK2	T2CK1	T2CK0	description
0	0	0	fx/512
0	0	1	fx/32
0	1	0	fx/16
0	1	1	fx/8
1	0	0	fx/4
1	0	1	fx/2
1	1	0	fx/1
1	1	1	External clock (EC2)

T2IFR When T2 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T2 Interrupt no generation

1 T2 Interrupt generation

RLD2EN Control Timer 2 Reload Signal

0 Enable Timer 2 reload signal

1 Disable Timer 2 reload signal

T2POL T2O/PWM2O Polarity Selection

0 Start High (T2O/PWM2O is low level at disable)

1 Start Low (T2O/PWM2O is high level at disable)

T2ECE Timer 2 External Clock Edge Selection

0 External clock falling edge

1 External clock rising edge

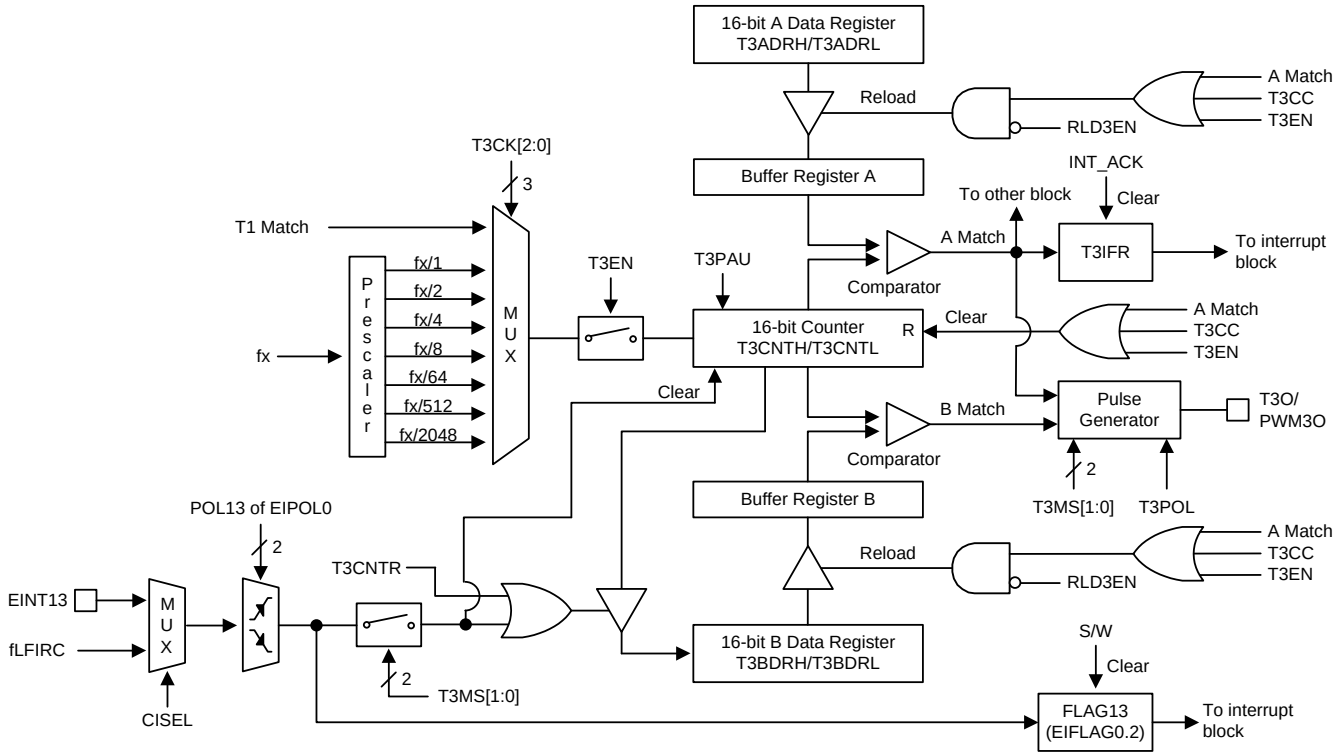
T2CNTR Timer 2 Counter Read Control

0 No effect

1 Load the counter value to the B data register (When write, automatically cleared “0” after being loaded)

10.8 TIMER 3

10.8.1 BLOCK DIAGRAM



Notes: 1. The T3EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. The RLD3EN bit should be “0b” when the T3EN bit is changed “0b” to “1b”.

16-Bit Timer Counter 3 Block Diagram

10.8.2 REGISTER MAP

Name	Address	Dir	Default	Description
T3CRH	CBH	R/W	00H	Timer 3 Control High Register
T3CRL	CAH	R/W	00H	Timer 3 Control Low Register
T3ADRH	CDH	R/W	FFH	Timer 3 A Data High Register
T3ADRL	CCH	R/W	FFH	Timer 3 A Data Low Register
T3BDRH	CFH	R/W	FFH	Timer 3 B Data High Register
T3BDRL	CEH	R/W	FFH	Timer 3 B Data Low Register

Register Map

10.8.3 REGISTER DESCRIPTION FOR TIMER 3

T3ADRH (Timer 3 A Data High Register) : CDH

.7	.6	.5	.4	.3	.2	.1	.0
T3ADRH7	T3ADRH6	T3ADRH5	T3ADRH4	T3ADRH3	T3ADRH2	T3ADRH1	T3ADRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T3ADRH[7:0] T3 A Data High Byte

T3ADRL (Timer 3 A Data Low Register) : CCH

.7	.6	.5	.4	.3	.2	.1	.0
T3ADRL7	T3ADRL6	T3ADRL5	T3ADRL4	T3ADRL3	T3ADRL2	T3ADRL1	T3ADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T3ADRL[7:0] T3 A Data Low Byte

T3BDRH (Timer 3 B Data High Register) : CFH

.7	.6	.5	.4	.3	.2	.1	.0
T3BDRH7	T3BDRH6	T3BDRH5	T3BDRH4	T3BDRH3	T3BDRH2	T3BDRH1	T3BDRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T3BDRH[7:0] T3 B Data High Byte

T3BDRL (Timer 3 B Data Low Register) : CEH

.7	.6	.5	.4	.3	.2	.1	.0
T3BDRL7	T3BDRL6	T3BDRL5	T3BDRL4	T3BDRL3	T3BDRL2	T3BDRL1	T3BDRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T3BDRL[7:0] T3 B Data Low Byte

T3CRH (Timer 3 Control High Register) : CBH

.7	.6	.5	.4	.3	.2	.1	.0
T3EN	–	T3MS1	T3MS0	CISEL	–	T3PAU	T3CC
R/W	–	R/W	R/W	R/W	–	R/W	R/W

Initial value: 00H

T3EN Control Timer 3

0 Timer 3 disable

1 Timer 3 enable (Counter clear and start)

T3MS[1:0] Control Timer 3 Operation Mode

T3MS1	T3MS0	description
0	0	Timer/counter mode (T3O: toggle at A match)
0	1	Capture mode (The A match interrupt can occur)
1	0	PPG one-shot mode (PWM3O)
1	1	PPG repeat mode (PWM3O)

CISEL Select Capture Input

0 EINT13

1 f_{LFIRC}

T3PAU Timer 3 Counter Temporary Pause Control

0 Continue counting

1 Temporary pause

T3CC Clear Timer 3 Counter

0 No effect

1 Clear the Timer 3 counter (When write, automatically cleared “0” after being cleared counter)

T3CRL (Timer 3 Control Low Register) : CAH

.7	.6	.5	.4	.3	.2	.1	.0
T3CK2	T3CK1	T3CK0	T3IFR	RLD3EN	T3POL	–	T3CNTR
R/W	R/W	R/W	R/W	R/W	R/W	–	R/W

Initial value: 00H

T3CK[2:0] Select Timer 3 clock source. fx is system clock frequency

T3CK2	T3CK1	T3CK0	description
0	0	0	fx/2048
0	0	1	fx/512
0	1	0	fx/64
0	1	1	fx/8
1	0	0	fx/4
1	0	1	fx/2
1	1	0	fx/1
1	1	1	T1 match

T3IFR When T3 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T3 Interrupt no generation

1 T3 Interrupt generation

RLD3EN Control Timer 3 Reload Signal

0 Enable Timer 3 reload signal

1 Disable Timer 3 reload signal

T3POL T3O/PWM3O Polarity Selection

0 Start High (T3O/PWM3O is low level at disable)

1 Start Low (T3O/PWM3O is high level at disable)

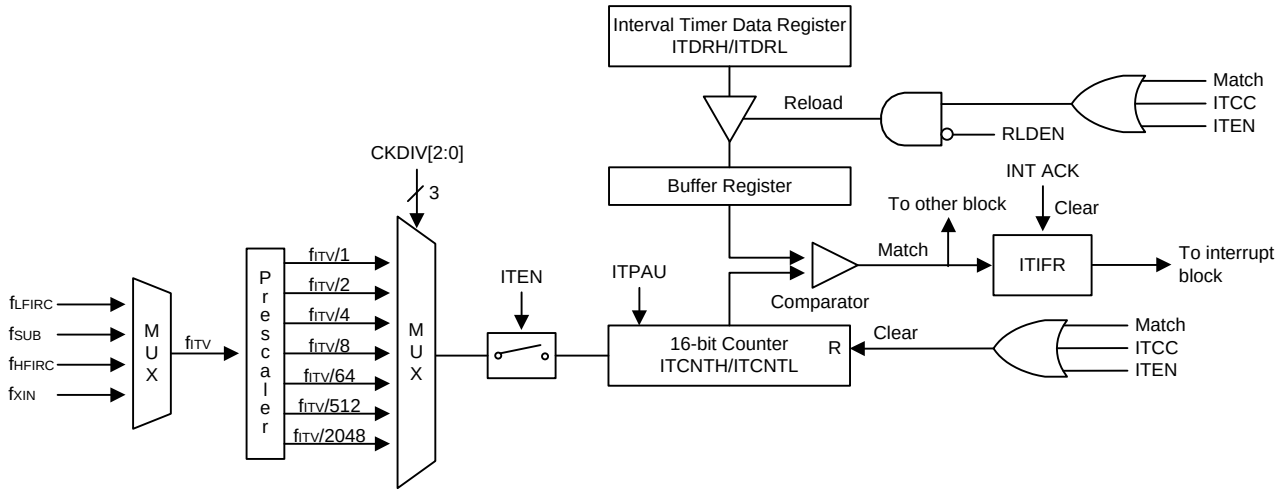
T3CNTR Timer 3 Counter Read Control

0 No effect

1 Load the counter value to the B data register (When write, automatically cleared “0” after being loaded)

10.9 16-BIT INTERVAL TIMER

10.9.1 BLOCK DIAGRAM



Notes: 1. The RLDEN bit should be “0b” when the ITEN bit is changed “0b” to “1b”..

16-Bit Interval Timer Block Diagram

10.9.2 REGISTER MAP

Name	Address	Dir	Default	Description
ITCRH	B6H	R/W	00H	Interval Timer Control High Register
ITCRL	B5H	R/W	00H	Interval Timer Control Low Register
ITDRH	AEH	R/W	FFH	Interval Timer Data High Register
ITDRL	ADH	R/W	FFH	Interval Timer Data Low Register

Register Map

10.9.3 REGISTER DESCRIPTION FOR INTERVAL TIMER

ITDRH (Interval Timer Data High Register) : AEH

.7	.6	.5	.4	.3	.2	.1	.0
ITDRH7	ITDRH6	ITDRH5	ITDRH4	ITDRH3	ITDRH2	ITDRH1	ITDRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

ITDRH[7:0] Interval Timer Data High Byte

ITDRL (Interval Timer Data Low Register) : ADH

.7	.6	.5	.4	.3	.2	.1	.0
ITDRL7	ITDRL6	ITDRL5	ITDRL4	ITDRL3	ITDRL2	ITDRL1	ITDRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

ITDRL[7:0] Interval Timer Data Low Byte

ITCRH (Interval Timer Control High Register) : B6H

.7	.6	.5	.4	.3	.2	.1	.0
ITEN	–	–	–	–	–	ITPAU	ITCC
R/W	–	–	–	–	–	R/W	R/W

Initial value: 00H

ITEN Control Interval Timer

0 Interval Timer disable

1 Interval Timer enable (Counter clear and start)

ITPAU Interval Timer Counter Temporary Pause Control

0 Continue counting

1 Temporary pause

ITCC Clear Interval Timer Counter

0 No effect

1 Clear the Interval Timer counter (When write, automatically cleared “0” after being cleared counter)

ITCRL (Interval Timer Control Low Register) : B5H

.7	.6	.5	.4	.3	.2	.1	.0
CKDIV2	CKDIV1	CKDIV0	ITIFR	RLDEN	–	CKSEL1	CKSEL0
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W

Initial value: 00H

CKDIV[2:0] Interval Timer Clock Divider

CKDIV2	CKDIV1	CKDIV0	description
0	0	0	f_{ITV}/2048
0	0	1	f_{ITV} /512
0	1	0	f_{ITV} /64
0	1	1	f_{ITV} /8
1	0	0	f_{ITV} /4
1	0	1	f_{ITV} /2
1	1	0	f_{ITV} /1
1	1	1	Not Used

ITIFR When Interval Timer Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 Interval Timer Interrupt no generation

1 Interval Timer Interrupt generation

RLDEN Control Interval Reload Signal

0 Enable Interval Timer reload signal

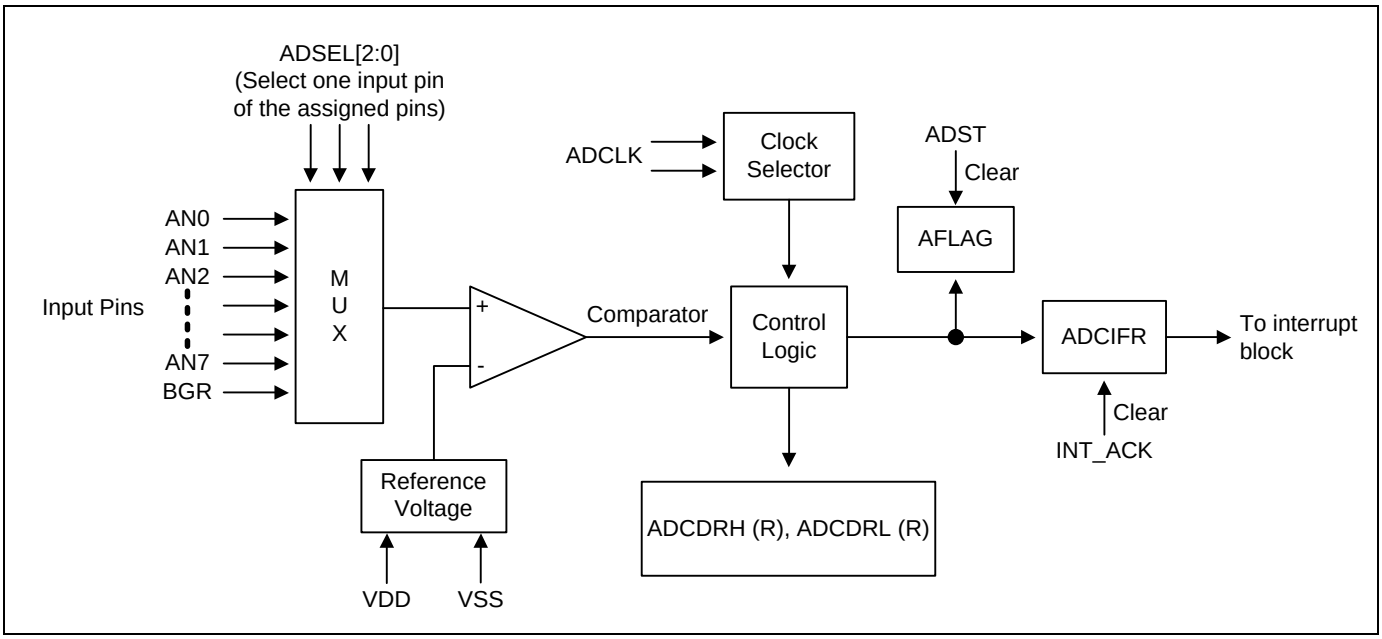
1 Disable Interval Timer reload signal

CKSEL[1:0] Select Interval Timer Clock

CKSEL1	CKSEL0	description
0	0	f_{LFIRC}
0	1	f_{SUB}
1	0	f_{HFIRC}
1	1	f_{XIN}

10.10 10-BIT A/D CONVERTER

10.10.1 BLOCK DIAGRAM



10-bit A/D Converter Block Diagram

10.10.2 REGISTER MAP

Name	Address	Dir	Default	Description
ADCCRH	9DH	R/W	00H	A/D Converter Control High Register
ADCCRL	9CH	R/W	00H	A/D Converter Control Low Register
ADCDRH	9FH	R	xxH	A/D Converter Data High Register
ADCDRL	9EH	R	xxH	A/D Converter Data Low Register

Register Map

10.10.3 REGISTER DESCRIPTION FOR A/D CONVERTR

ADCDRH (A/D Converter Data High Register) : 9FH

.7	.6	.5	.4	.3	.2	.1	.0
ADDM9	ADDM8	ADDM7	ADDM6	ADDM5	ADDM4	ADDM3 ADDL9	ADDM2 ADDL8
R	R	R	R	R	R	R	R

Initial value: xxH

ADDM[11:4] MSB align, A/D Converter High Result (8bit)

ADDL[11:8] LSB align, A/D Converter High Result (4bit)

ADCDRL (A/D Converter Data Low Register) : 9EH

.7	.6	.5	.4	.3	.2	.1	.0
ADDM1 ADDL7	ADDM0 ADDL6	ADDL5	ADDL4	ADDL3	ADDL2	ADDL1	ADDL0
R	R	R	R	R	R	R	R

Initial value: xxH

ADDM[3:0] MSB align, A/D Converter Low Result (4bit)

ADDL[7:0] LSB align, A/D Converter Low Result (8bit)

ADCCRH (A/D Converter Control High Register) : 9DH

.7	.6	.5	.4	.3	.2	.1	.0
ADCIFR	–	–	–	–	ALIGN	CKSEL1	CKSEL0
R/W	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

ADCIFR When ADC Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 ADC Interrupt no generation

1 ADC Interrupt generation

ALIGN A/D Converter Data Align Selection

0 MSB align; ADCDRH[7:0], ADCDRL[7:6]

1 LSB align; ADCDRH[1:0], ADCDRL[7:0]

CKSEL[1:0] A/D Converter Clock Selection

CKSEL1	CKSEL0	description
0	0	fx/1
0	1	fx/2
1	0	fx/4
1	1	fx/8

ADCCRL (A/D Converter Control Low Register): 9CH

.7	.6	.5	.4	.3	.2	.1	.0
STBY	ADST	–	AFLAG	ADSEL3	ADSEL2	ADSEL1	ADSEL0
R/W	R/W	–	R	R/W	R/W	R/W	R/W

Initial value: 00H

STBY Control Operation of A/D

(The ADC module is automatically disabled at stop mode)

0 ADC module disable

1 ADC module enable

ADST Control A/D Conversion Start

0 No effect

1 ADC conversion start and auto clear

AFLAG A/D Converter Operation State (This bit is cleared to '0' when the STBY bit is set to '0' or when the CPU is at stop mode.)

0 During A/D Conversion

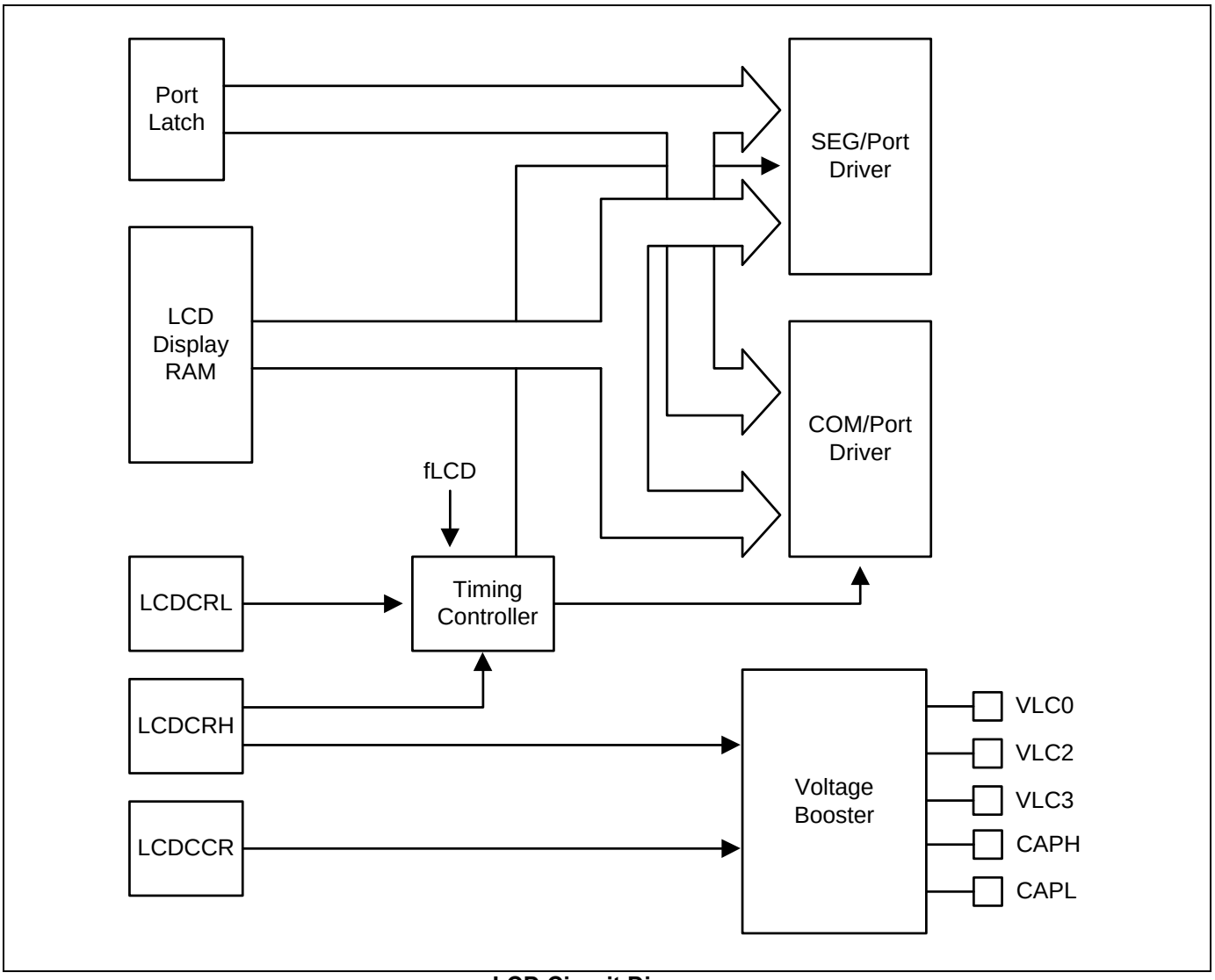
1 A/D Conversion finish

ADSEL[3:0] A/D Converter Channel Selection

ADSEL3	ADSEL2	ADSEL1	ADSEL0	description
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	1	1	1	V_{BGR} (about 1.21V)

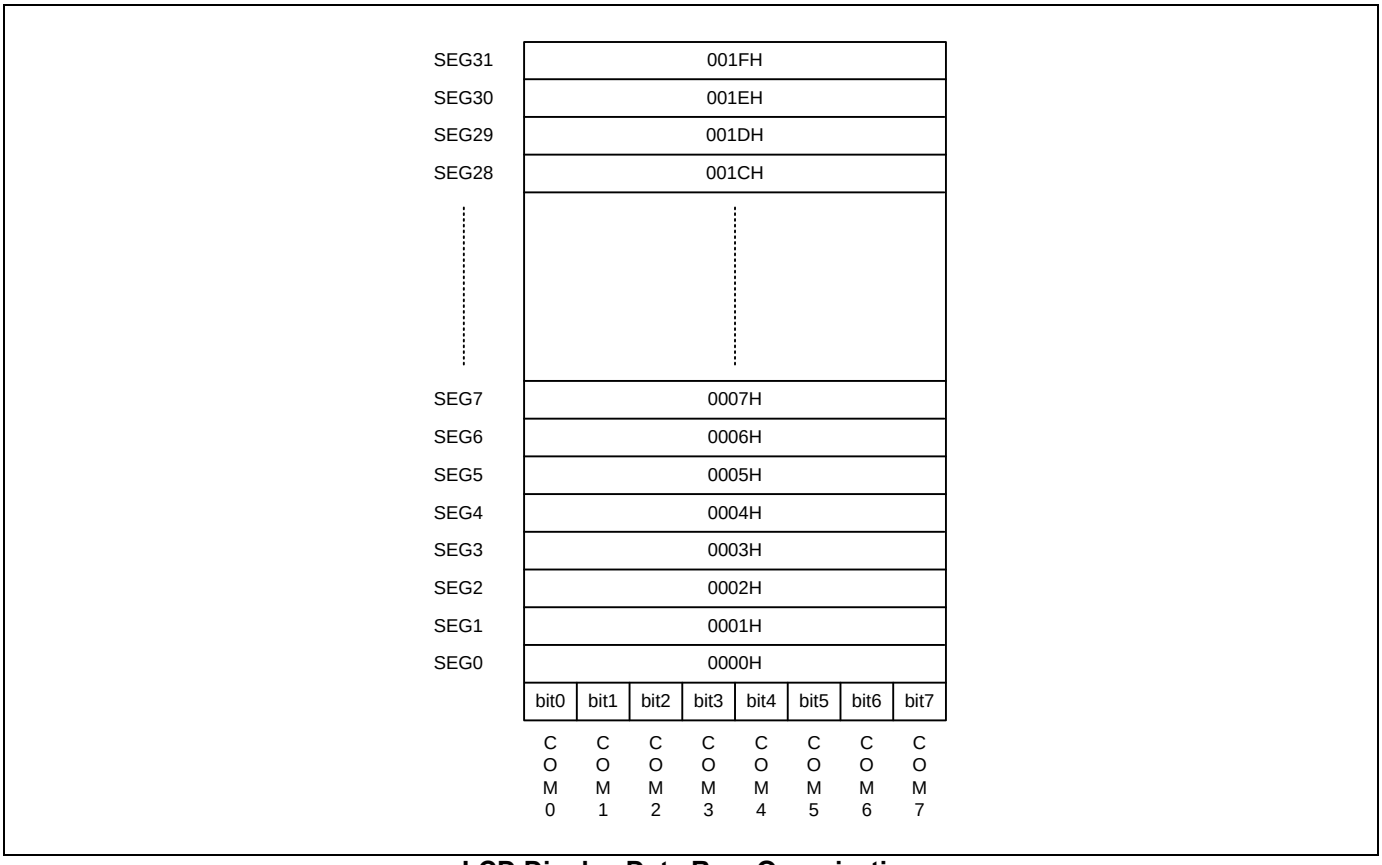
10.11 LCD DRIVER

10.11.1 BLOCK DIAGRAM



LCD Circuit Diagram

10.11.2 LCD DISPLAY RAM ORGANIZATION



LCD Display Data Ram Organization

10.11.3 REGISTER MAP

Name	Address	Dir	Default	Description
LCDBLCR	91H	R/W	00H	LCD Back Light Control Register
LCDCRL	99H	R/W	00H	LCD Driver Control Low Register
LCDCRH	9AH	R/W	00H	LCD Driver Control High Register
LCDCCR	9BH	R/W	00H	LCD Driver Contrast Control Register

Register Map

10.11.4 REGISTER DESCRIPTION FOR LCD DRIVER

LCDCRH (LCD Driver Control High Register) : 9AH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	BTYPE1	BTYPE0	DISP
–	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

BTYPE[1:0] LCD Bias Type Select

BTYPE1	BTYPE0	description
0	0	Internal resistor bias
0	1	External resistor bias
1	0	Capacitor bias (Voltage booster)
1	1	Not available

Notes:

1. All the VLC0, VLC2, VLC3, CAPH, and CAPL pins must be used as bias functions (P5FSR.4-.0 = “11111b”) when the capacitor bias is selected for the LCD bias type.
2. Refer to the P5FSR register for pin functions.

DISP LCD Display Control

0 Display off (The LCD block and voltage booster are off)

1 Normal display on (When the BTYPE[1:0] = “10b”, the voltage booster is turn on)

LCDCRL (LCD Driver Control Low Register) : 99H

.7	.6	.5	.4	.3	.2	.1	.0
IRSEL1	IRSEL0	–	DBS2	DBS1	DBS0	LCLK1	LCLK0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IRSEL Internal LCD Bias Dividing Resistor Select

IRSEL1	IRSEL0	
0	0	RLCD = 60kΩ (R_{LCD2})
0	1	RLCD = 30kΩ (R_{LCD1})
1	0	RLCD = 120kΩ (R_{LCD3})
1	1	Not available

DBS[2:0] LCD Duty and Bias Select

DBS2	DBS1	DBS0	description	
BTYPE[1:0]		=	"00b"	"01b" or "10b"
0	0	0	1/8 duty, 1/4 bias,	1/8 duty, 1/3 bias
0	0	1	1/6 duty, 1/4 bias,	1/6 duty, 1/3 bias
0	1	0	1/5 duty, 1/3 bias,	1/5 duty, 1/3 bias
0	1	1	1/4 duty, 1/3 bias,	1/4 duty, 1/3 bias
1	0	0	1/3 duty, 1/3 bias,	1/3 duty, 1/3 bias
1	0	1	1/3 duty, 1/2 bias,	1/3 duty, 1/2 bias
1	1	0	1/2 duty, 1/2 bias,	1/2 duty, 1/2 bias
1	1	1	Not available	

Note: The LCD bias is changed as 1/3 bias on 1/8 and 1/6 duty when the external resistor and capacitor bias is selected by BTYPE[1:0] bits ("01b" or "10b").

LCLK[1:0] LCD Clock Select (When fwck(Watch timer clock)=32.768kHz)

LCLK1	LCLK0	description
0	0	fLCD = 128Hz
0	1	fLCD = 256Hz
1	0	fLCD = 512Hz
1	1	fLCD = 1024Hz

Note: The LCD clock is generated by watch timer clock (f_{WCK}). So the watch timer should be enabled when the LCD display is turned on.

LCDCCR (LCD Driver Contrast Control Register) : 9BH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	VLCD3	VLCD2	VLCD1	VLCD0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

VLCD[3:0] VLCD3 Voltage Control when the capacitor bias is selected

VLCD3	VLCD2	VLCD1	VLCD0		Description 1/2 Bias	1/3 Bias
0	0	0	0	VLC3 =	1.00V	0.75V
0	0	0	1	VLC3 =	1.05V	0.79V
0	0	1	0	VLC3 =	1.10V	0.83V
0	0	1	1	VLC3 =	1.15V	0.86V
0	1	0	0	VLC3 =	1.20V	0.90V
0	1	0	1	VLC3 =	1.25V	0.94V
0	1	1	0	VLC3 =	1.30V	0.98V
0	1	1	1	VLC3 =	1.35V	1.01V
1	0	0	0	VLC3 =	1.40V	1.05V
1	0	0	1	VLC3 =	1.45V	1.09V
1	0	1	0	VLC3 =	Not available	Not available
1	0	1	1	VLC3 =	Not available	Not available
1	1	0	0	VLC3 =	Not available	Not available
1	1	0	1	VLC3 =	Not available	Not available
1	1	1	0	VLC3 =	Not available	Not available
1	1	1	1	VLC3 =	Not available	Not available

Note) The VLCD1 voltage can be calculated by the below formulas.

- VLC0 = VLC3 x 2 ; 1/2 bias
- VLC0 = VLC3 x 3 ; 1/3 bias

LCDBLCR (LCD Back Light Control Register) : 91H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	DRV11	DRV10	DRV01	DRV00
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

DRV1[1:0] Select LCD Back Light Drive Current on LCDBL1 Pin

DRV11	DRV10	description
0	0	IOL=10mA at 3V and VOL=1V
0	1	IOL=20mA at 3V and VOL=1V
1	0	IOL=30mA at 3V and VOL=1V
1	1	Not available

Notes:

1. To use the LCD back light drive current, the P37/LCDBL1 pin should be selected for the LCD back light function by the P3FSRH.7-6 = “11b”.
2. Refer to the P3FSRH register for pin functions.

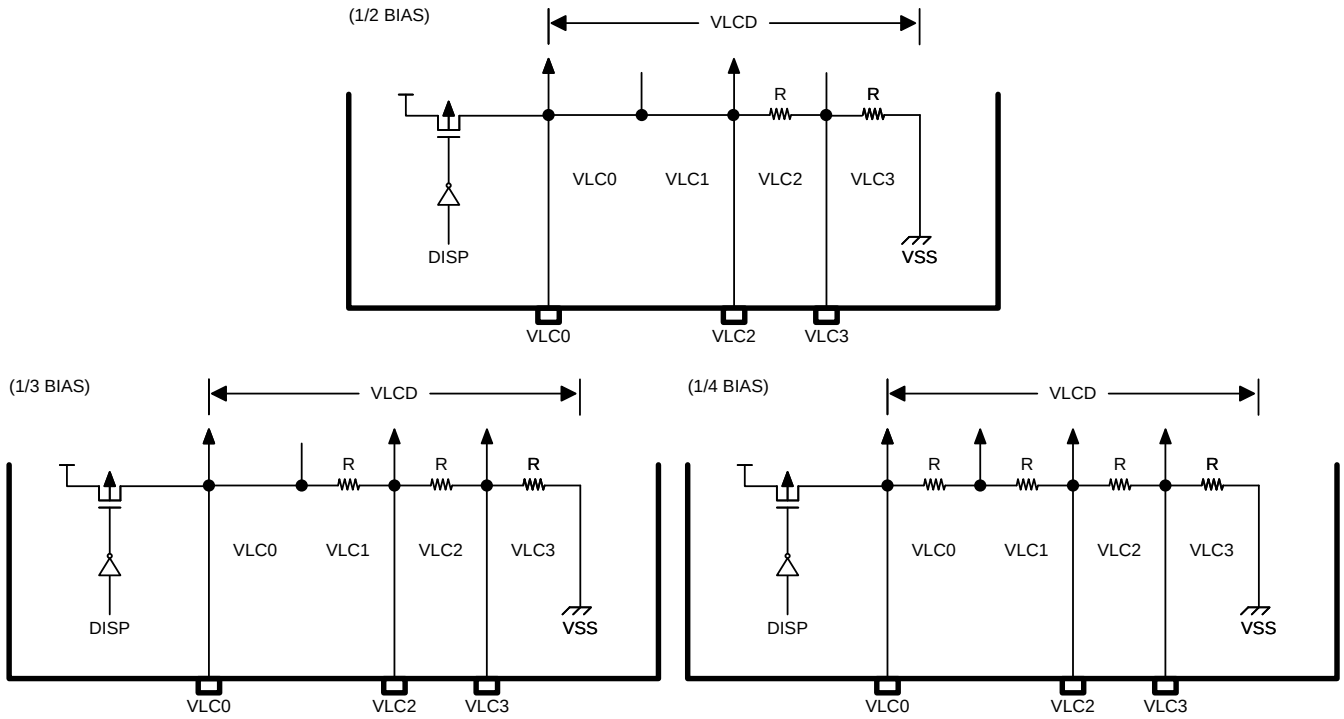
DRV0[1:0] Select LCD Back Light Drive Current on LCDBL0 Pin

DRV11	DRV10	description
0	0	IOL=10mA at 3V and VOL=1V
0	1	IOL=20mA at 3V and VOL=1V
1	0	IOL=30mA at 3V and VOL=1V
1	1	Not available

Notes:

1. To use the LCD back light drive current, the P36/LCDBL0 pin should be selected for the LCD back light function by the P3FSRH.5-4 = “11b”.
2. Refer to the P3FSRH register for pin functions.

10.11.5 INTERNAL RESISTOR BIAS CONNECTON

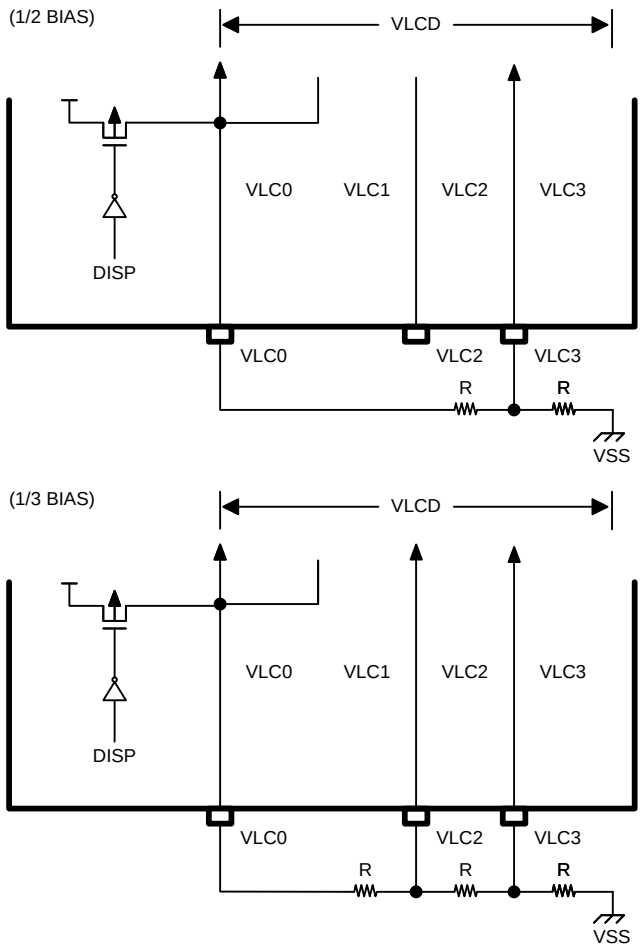


Notes:

1. When 1/2 bias are selected, the VLC0, VLC1, and VLC2 are internally connected.
2. When 1/3 bias are selected, the VLC0 and VLC1 are internally connected.
3. When the internal resistors are selected, all the P50/VLC0, P51/VLC2, P52/VLC3, P53/CAPH, and P54/CAPL pins can be used for normal I/O.

Internal Resistor Bias Connection

10.11.6 EXTERNAL RESISTOR BIAS CONNECTON

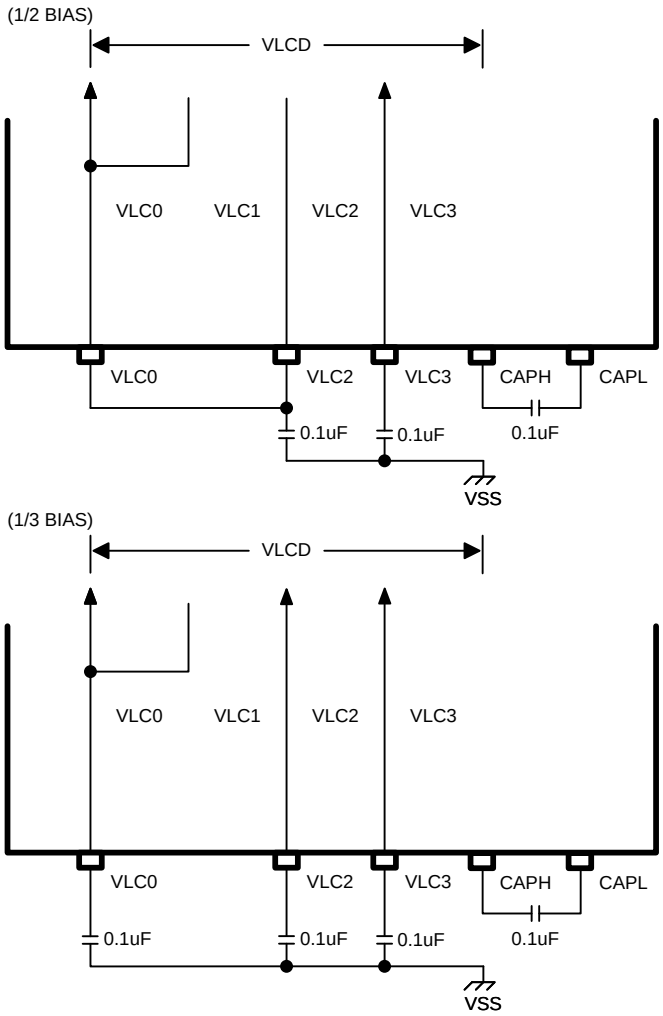


Notes:

1. When the external resistor bias is selected, the internal resistors for bias are disconnected.
2. When the external resistor bias is selected, the dividing resistors should be connected like the above figure and the needed bias pins should be selected as the LCD bias function pins (VLC0, VLC2, and VLC3) by P5FSR register.
   - When it is 1/2 bias, the P50/VLC0 and P52/VLC3 pins should be selected as VLC0 and VLC3 functions. The P51/VLC2 pin can be used for normal I/O.
   - When it is 1/3 bias, the P50/VLC0, P51/VLC2, and P52/VLC3 pins should be selected as VLC0, VLC2, and VLC3 functions.

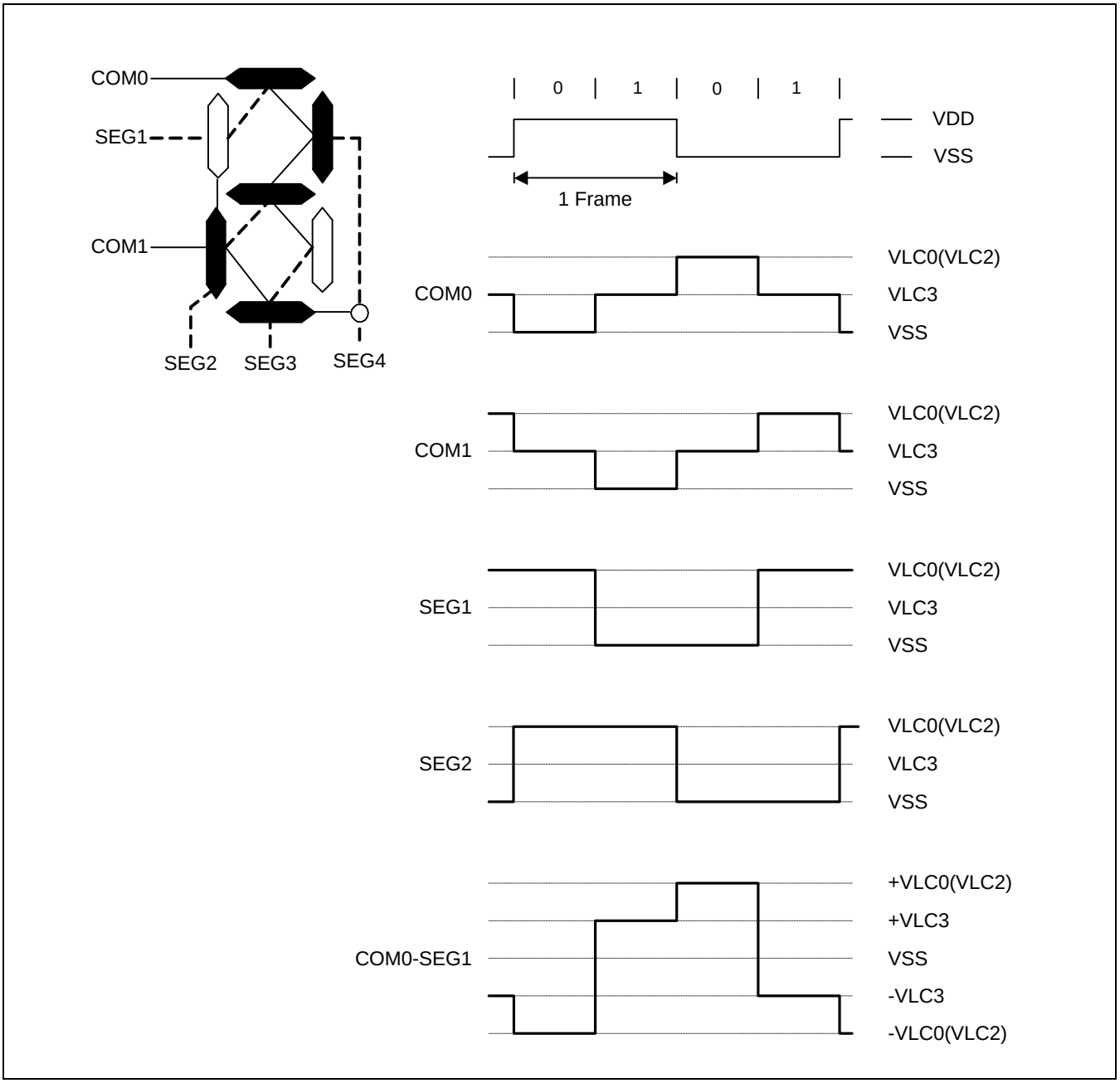
External Resistor Bias Connection

10.11.7 CAPACITOR BIAS CONNECTION

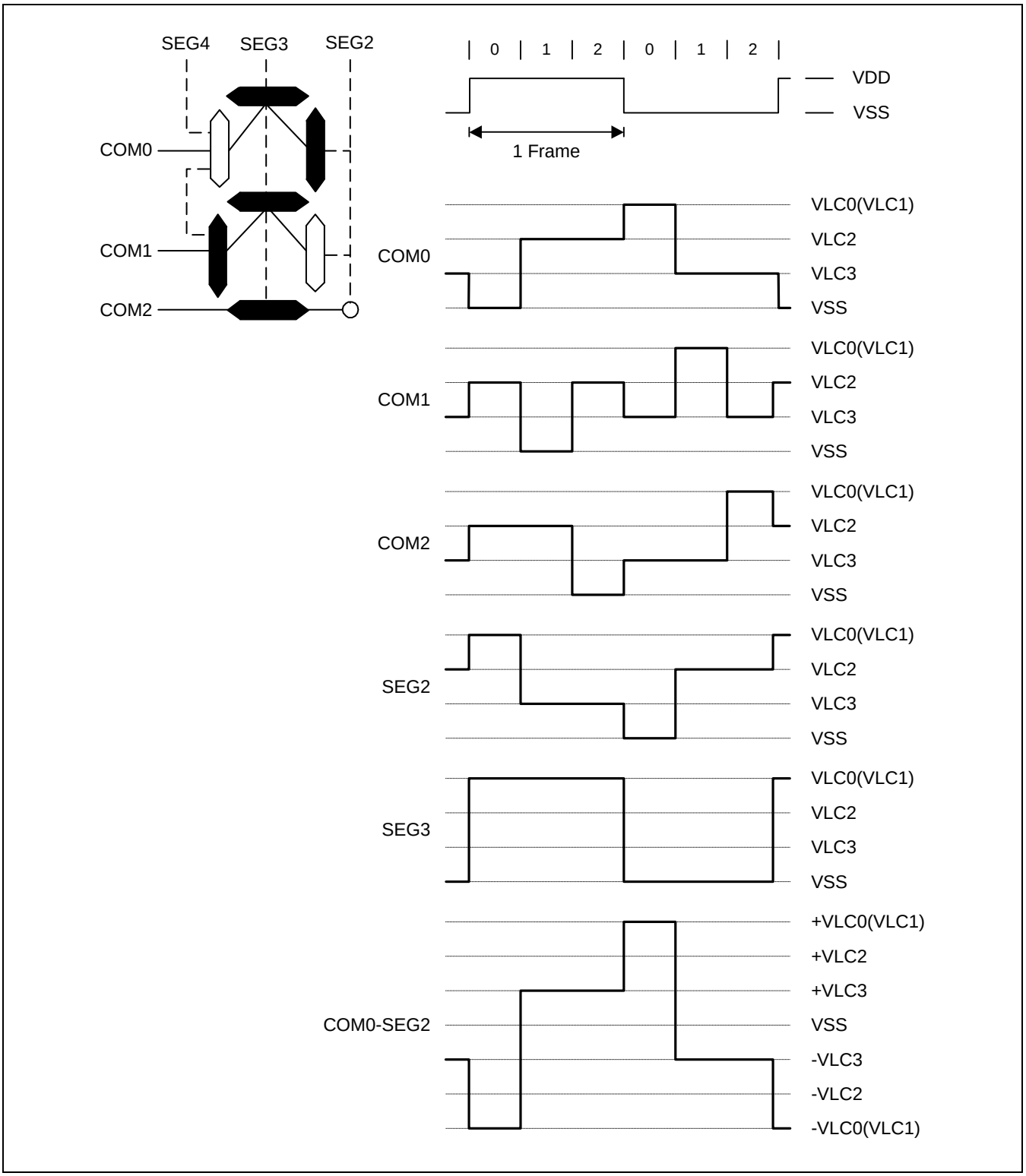


Note: When the capacitor bias is selected for the VLCD voltage, all the P50/VLC0, P51/VLC2, P52/VLC3, P53/CAPH, and P54/CAPL pins should be selected for LCD bias function pins by the P5FSR and should be connected like the above figure.

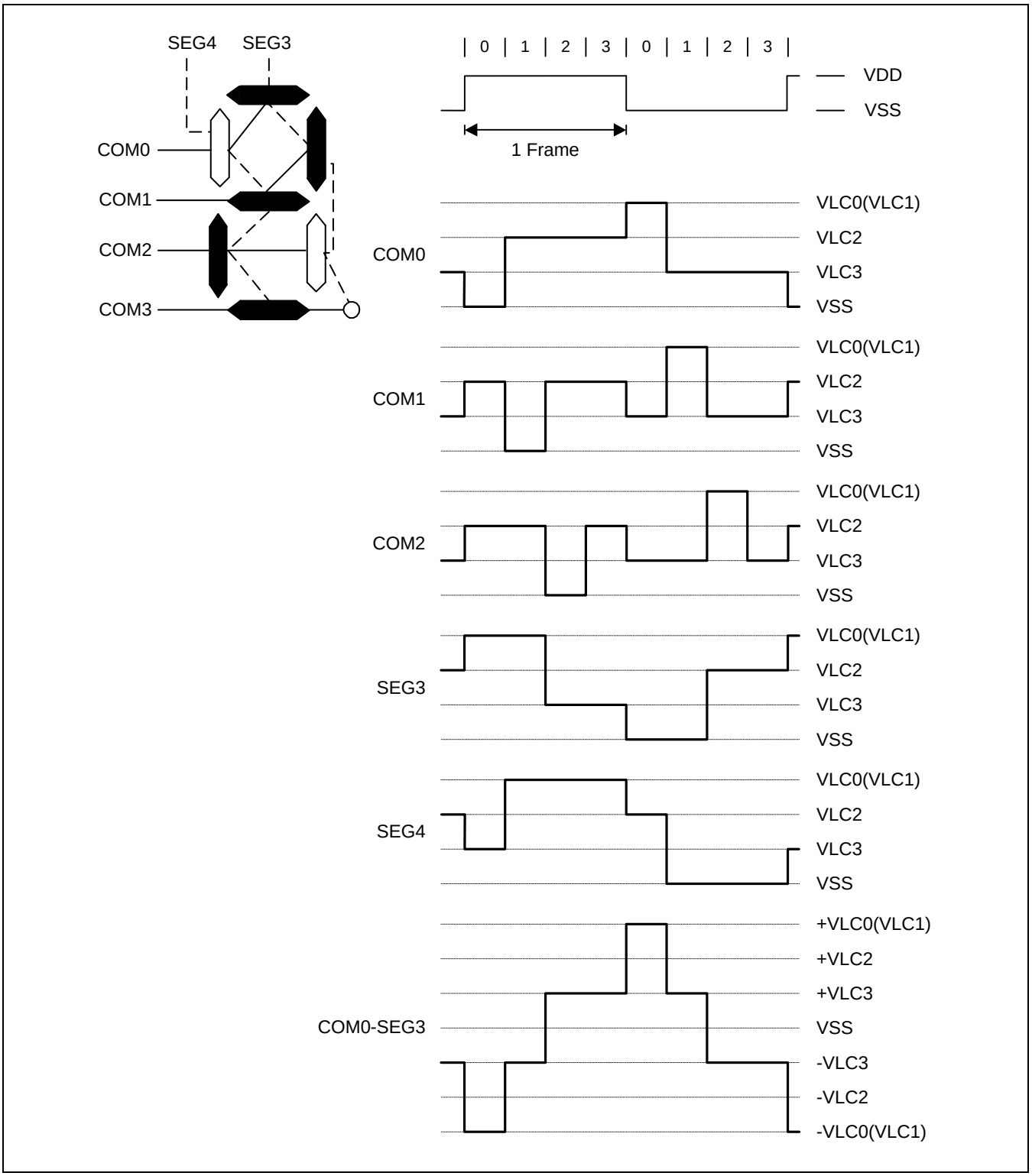
Capacitor Bias Connection



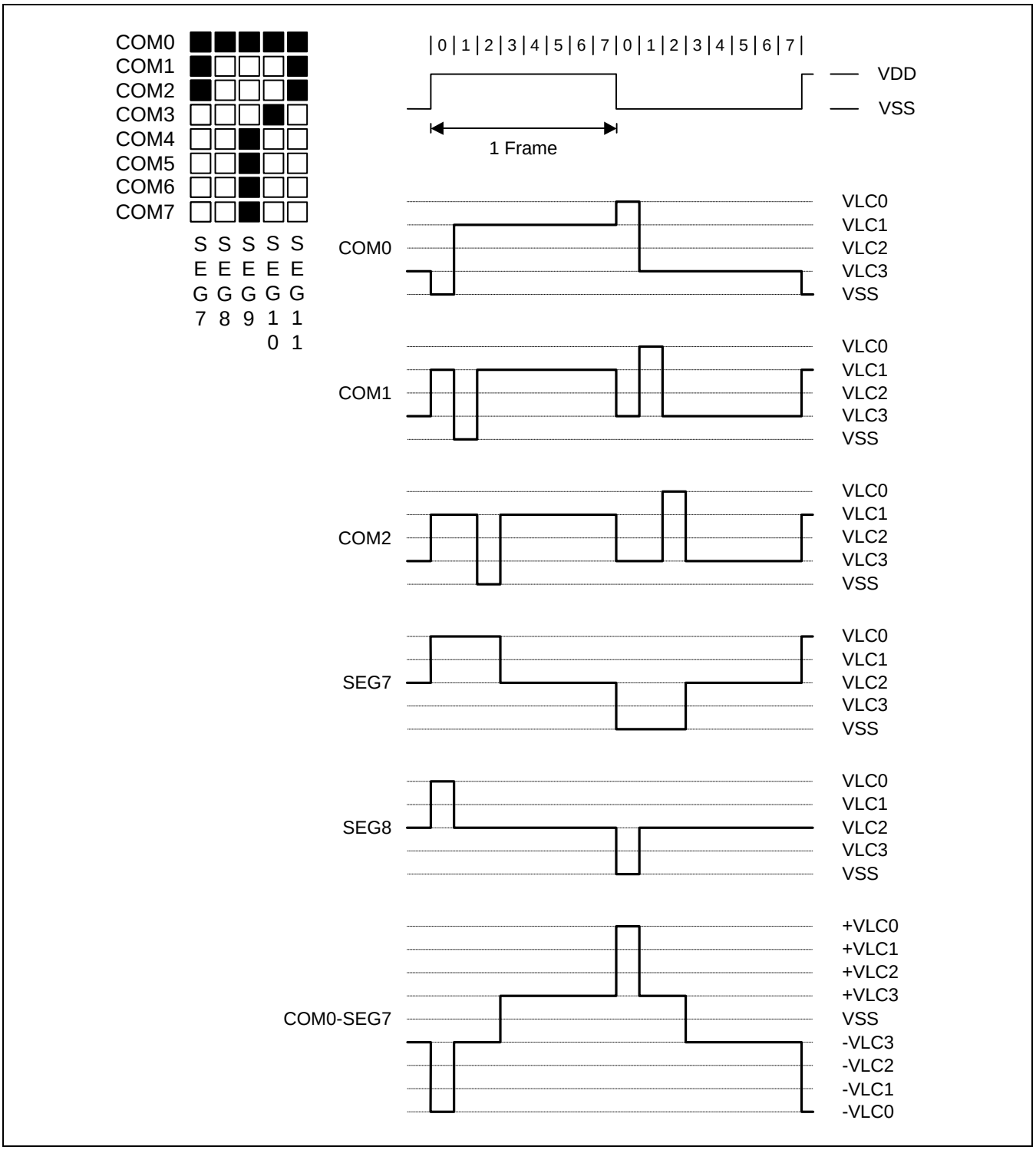
LCD Signal Waveforms (1/2 Duty, 1/2 Bias)



LCD Signal Waveforms (1/3 Duty, 1/3 Bias)



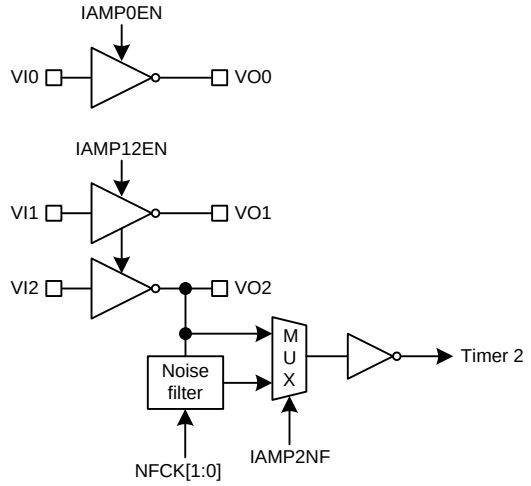
LCD Signal Waveforms (1/4 Duty, 1/3 Bias)



LCD Signal Waveforms (1/8 Duty, 1/4 Bias)

10.12 INVERTER AMPLIFIER

10.12.1 BLOCK DIAGRAM



Note: The VI1, VO1, VI2, and VO2 pins should be set to the corresponding functions by P3FSRH/L registers during the Inverter amplifier 1/2 is enabled by IAMPCR.IAMP12EN bit

Inverter Amplifier 0/1/2 Block Diagram

10.12.2 REGISTER MAP

Name	Address	Dir	Default	Description
IAMPCR	E1H	R/W	00H	Inverter Amplifier Control Register

Register Map

10.12.3 REGISTER DESCRIPTION FOR AMPLIFIER

IAMPCR (Inverter Amplifier 0 Control Register) : E1H

.7	.6	.5	.4	.3	.2	.1	.0
IAMP2NF	–	NFCK1	NFCK0	–	–	IAMP12EN	IAMP0EN
R/W	–	R/W	R/W	–	–	R/W	R/W

Initial value: 00H

IAMP2NF Configure Noise filter of Inverter Amplifier 2

0 Disable

1 Enable

NFCK[1:0] Comparator Noise Filter Sampling Clock Selection

NFCK1	NFCK0	description
0	0	fx/1
0	1	fx/4
1	0	fx/16
1	1	fx/64

IAMP12EN Control operation of inverter amplifier 1/2

0 Disable inverter amplifier 1/2

1 Enable inverter amplifier 1/2

IAMP0EN Control operation of inverter amplifier 0

0 Disable inverter amplifier 0

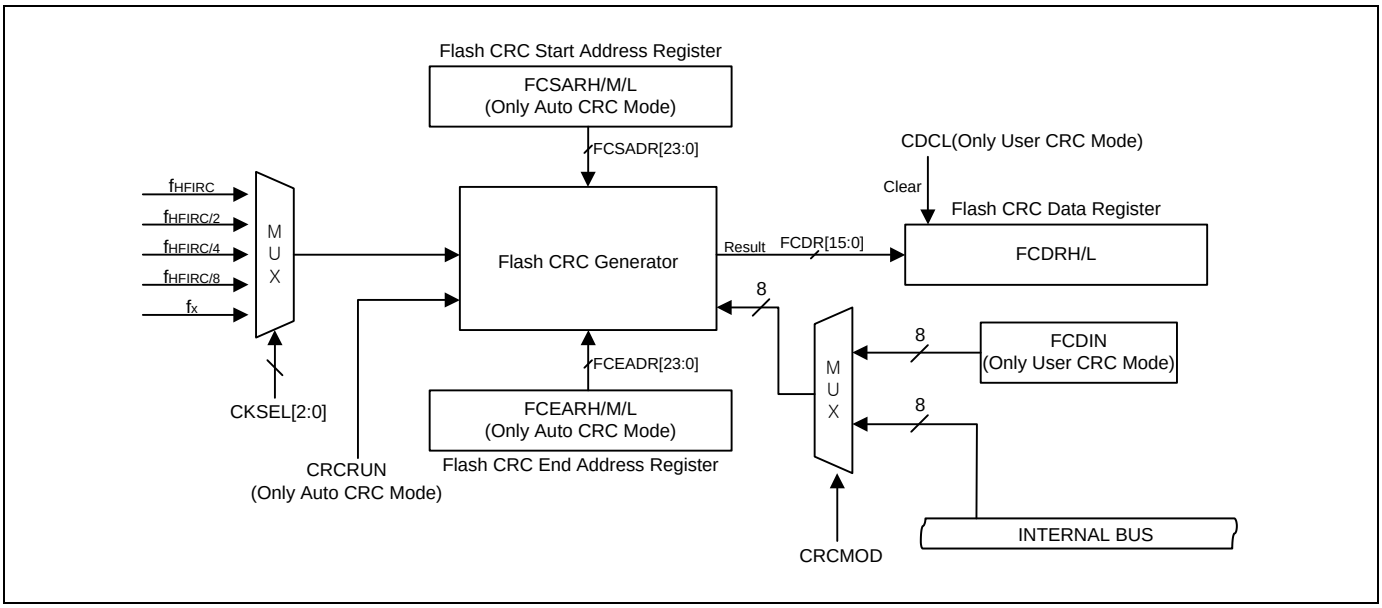
1 Enable inverter amplifier 0

Notes:

1. If a level is not detected on an enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clocks or more to be actually detected as a valid edge.

10.13 FLASH CRC GENERATOR

10.13.1 BLOCK DIAGRAM



10.13.2 REGISTER MAP

Name	Address	Dir	Default	Description
FCSARH	5050H (ESFR)	R/W	00H	Flash CRC Start Address High Register
FCEARH	5051H (ESFR)	R/W	00H	Flash CRC End Address High Register
FCSARM	5052H (ESFR)	R/W	00H	Flash CRC Start Address Middle Register
FCEARM	5053H (ESFR)	R/W	00H	Flash CRC End Address Middle Register
FCSARL	5054H (ESFR)	R/W	00H	Flash CRC Start Address Low Register
FCEARL	5055H (ESFR)	R/W	00H	Flash CRC End Address Low Register
FCCR	5056H (ESFR)	R/W	00H	Flash CRC Control Register
FCDRH	5057H (ESFR)	R	FFH	Flash CRC Data High Register
FCDRL	5058H (ESFR)	R	FFH	Flash CRC Data Low Register
FCDIN	AFH	R/W	00H	Flash CRC Data In Register

Register Map

10.13.3 REGISTER DESCRIPTION FOR FLASH CRC GENERATOR

FCSARH (Flash CRC Start Address High Register) : 5050H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	–	–	FCSARH0
–	–	–	–	–	–	–	R/W

Initial value: 00H

FCSARH[7:0] Flash CRC Start Address High
Note) Used only to Auto CRC Mode

FCSARM (Flash CRC Start Address Middle Register) : 5052H

.7	.6	.5	.4	.3	.2	.1	.0
FCSARM7	FCSARM6	FCSARM5	FCSARM4	FCSARM3	FCSARM2	FCSARM1	FCSARM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FCSARM[7:0] Flash CRC Start Address Middle
Note) Used only to Auto CRC Mode

FCSARL (Flash CRC Start Address Low Register) : 5054H

.7	.6	.5	.4	.3	.2	.1	.0
FCSARL7	FCSARL6	FCSARL5	FCSARL4	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–

Initial value: 00H

FCSARL[7:0] Flash CRC Start Address Low
Note) Used only to Auto CRC Mode

FCEARH (Flash CRC End Address High Register) : 5051H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	–	–	FCEARH0
–	–	–	–	–	–	–	R/W

Initial value: 00H

FCEARH[7:0] Flash CRC End Address High
Note) Used only to Auto CRC Mode

FCEARM (Flash CRC End Address Middle Register) : 5053H

.7	.6	.5	.4	.3	.2	.1	.0
FCEARM7	FCEARM6	FCEARM5	FCEARM4	FCEARM3	FCEARM2	FCEARM1	FCEARM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FCEARM[7:0] Flash CRC End Address Middle
Note) Used only to Auto CRC Mode

FCEARL (Flash CRC End Address Low Register) : 5055H

.7	.6	.5	.4	.3	.2	.1	.0
FCEARL7	FCEARL6	FCEARL5	FCEARL4	1	1	1	1
R/W	R/W	R/W	R/W	–	–	–	–

Initial value: 00H

FCEARL [7:0] Flash CRC End Address Low
Note) Used only to Auto CRC Mode

FCDRH (Flash CRC Data High Register) : 5057H

.7	.6	.5	.4	.3	.2	.1	.0
FCDRH7	FCDRH6	FCDRH5	FCDRH4	FCDRH3	FCDRH2	FCDRH1	FCDRH0
R	R	R	R	R	R	R	R

Initial value: FFH

FCDRH [7:0] Flash CRC Data High

FCDRL (Flash CRC Data Low Register) : 5058H

.7	.6	.5	.4	.3	.2	.1	.0
FCDRL7	FCDRL6	FCDRL5	FCDRL4	FCDRL3	FCDRL2	FCDRL1	FCDRL0
R	R	R	R	R	R	R	R

Initial value: FFH

FCDRL [7:0] Flash CRC Data Low

FCDIN (Flash CRC Data IN Register) : D7H

.7	.6	.5	.4	.3	.2	.1	.0
FCDIN7	FCDIN6	FCDIN5	FCDIN4	FCDIN3	FCDIN2	FCDIN1	FCDIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FCDIN [7:0] Flash CRC Data In
Note) Used only to User CRC Mode

FCCR (Flash CRC Control Register) : 5056H

.7	.6	.5	.4	.3	.2	.1	.0
CRCMOD	CDCL	MDSEL	–	CKSEL2	CKSEL1	CKSEL0	CRCRUN
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

Initial value: 00H

CRCMOD Select CRC/Checksum Mode

0 Auto CRC/Checksum Mode
1 User CRC/Checksum Mode

CDCL Flash CRC Data register Clear

0 No effect
1 Clear Flash CRC Data register

NOTE) This bit is cleared to '0' automatically after Flash CRC Data register is cleared. The FCDRH/L is set to "FFH" if the MDSEL is set to "0b" and "00H" if the MDSEL is set to "1b". Used only to User CRC/Checksum Mode.

MDSEL CRC/Checksum Selection

0 Select CRC
1 Select Checksum

CKSEL[2:0] Select Flash CRC/Checksum Clock

CKSEL2	CKSEL1	CKSEL0	description
0	0	0	f_{HFIRC}
0	0	1	$f_{HFIRC}/2$
0	1	0	$f_{HFIRC}/4$
0	1	1	$f_{HFIRC}/8$
1	0	0	fx (system clock)
Other Values			Not used

CRCRUN CRC/Checksum Start Signal & Busy Flag, Used only to Auto CRC/Checksum mode

0 Indicates that CRC/Checksum operation is not running or has finished. When written "0", CRC/Checksum operation is finished by force even if CRC/Checksum operation is running. It has no effect to write "0" if CRC/Checksum is not running currently.
1 When written "1", CRC/Checksum operation starts and this bit remains "1" as long as CRC/Checksum operation is on-going. This bit is cleared to "0" automatically after CRC/Checksum operation finishes.

Note: If f_{HFIRC}, $f_{HFIRC}/2$, $f_{HFIRC}/4$, and $f_{HFIRC}/8$ is selected,HFIRCE must be cleared to '0' at OSCCR.

11. POWER DOWN OPERATION

11.1 POWER DOWN MODE

11.1.1 REGISTER MAP

Name	Address	Dir	Default	Description
PCON	87H	R/W	00H	Power Control Register
LVICR	86H	R/W	00H	Low Voltage Indicator Control Register
RSTFR	E8H	R/W	80H	Reset Flag Register
LVRCR	D8H	R/W	00H	Low Voltage Reset Control Register

Register Map

11.1.2 REGISTER DESCRIPTION

PCON (Power Control Register) : 87H

.7	.6	.5	.4	.3	.2	.1	.0
PCON7	–	–	–	PCON3	PCON2	PCON1	PCON0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

PCON[7:0]	Power control	
	01H	Enable Idle mode
	03H	Enable STOP mode
	Other Values	Normal operation

Notes: 1. To enter Idle mode, PCON must be set to ‘01H’.
2. To enter STOP mode, PCON must be set to ‘03H’.
3. The PCON register is automatically cleared by a release signal in STOP/Idle mode.
4. Three or more NOP instructions must immediately follow the instruction that make the device enter STOP/IDLE mode. Refer to the following examples

```
Ex1)  MOV   PCON, #01H   ; Idle mode
      NOP
      NOP
      NOP
       •
       •
       •
```

```
Ex2)  MOV   PCON, #03H   ; STOP mode
      NOP
      NOP
      NOP
       •
       •
       •
```

RSTFR (Reset Flag Register) : E8H

.7	.6	.5	.4	.3	.2	.1	.0
PORF	EXTRF	WDTRF	OCDRF	LVRF	–	–	–
R/W	R/W	R/W	R/W	R/W	–	–	–

Initial value: 80H

PORF Power-On Reset flag bit. This bit is reset by writing '0' to this bit.

0 No detection

1 Detection

EXTRF External Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

WDTRF Watch Dog Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

OCDRF On-Chip Debug Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

LVRF Low Voltage Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

Notes:

1. When the Power-On Reset occurs, the PORF bit is only set to "1", the other flag (WDTRF and OCDRF) bits are all cleared to "0".
2. When the Power-On Reset occurs, the EXTRF bit is unknown, At that time, the EXTRF bit can be set to "1" when External Reset (RESETB) occurs.
3. When the Power-On Reset occurs, the LVRF bit is unknown, At that time, the LVRF bit can be set to "1" when LVR Reset occurs.
4. When a reset except the POR occurs, the corresponding flag bit is only set to "1", the other flag bits are kept in the previous values.

LVRCR (Low Voltage Reset Control Register) : D8H

.7	.6	.5	.4	.3	.2	.1	.0
LVRST	–	–	–	–	LVRVS1	LVRVS0	LVREN
R/W	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

LVRST LVR Enable When Stop Release

0 Not effect at stop release

1 LVR enable at stop release

Notes:

1. When this bit is '1', the LVREN bit is cleared to '0' by stop release. (LVR enable)
2. When this bit is '0', the LVREN bit is not effect by stop release.

LVRVS[1:0] LVR Voltage Select

LVRVS1	LVRVS0	Description
0	0	1.62V
0	1	2.00V
1	0	2.40V
1	1	2.68V

LVREN LVR Operation

0 LVR Enable

1 LVR Disable

Notes:

1. The LVRVS[1:0] bits are cleared by a power-on reset but are retained by other reset signals.
2. The LVRVS[1:0] bits should be set to '0000b' while LVREN bit is "1".

LVICR (Low Voltage Indicator Control Register) : 86H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	LVIIFR	LVIEN	–	–	LVILS1	LVILS0
–	–	R/W	R/W	–	–	R/W	R/W

Initial value: 00H

LVIIFR When Low Voltage Indicator Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 No detection

1 Detection

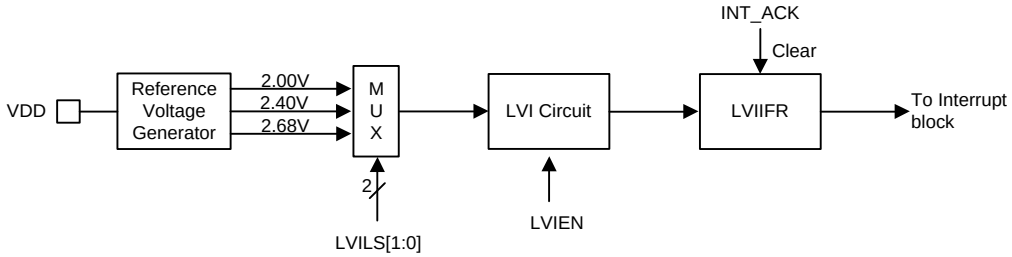
LVIEN LVI Enable/disable

0 Disable

1 Enable

LVILS[1:0] LVI Level Select

LVILS1	LVILS0	Description
0	0	2.00V
0	1	2.40V
1	0	2.68V



Notes:
1. The LVIIFR bit will be set to “1b” if the VDD goes down lower than a selected LVI level during LVIEN=”1b”.
2. The LVIIFR bit won’t be set to “1b” if the bit is cleared to “0b” during the VDD remains the lower voltage than the LVI level.
3. The LVIIFR bit may be set to “1b” if the LVIEN bit is set to “1b” again after the LVIEN bit is cleared to “0b” during VDD < the selected LVI level.

LVI Block Diagram

12. MEMORY PROGRAMMING

12.1 FLASH CONTROL AND STATUS REGISTER

12.1.1 REGISTER MAP

Name	Address	Dir	Default	Description
FSADRH	FAH	R/W	00H	Flash Sector Address High Register
FSADRM	FBH	R/W	00H	Flash Sector Address Middle Register
FSADRL	FCH	R/W	00H	Flash Sector Address Low Register
FIDR	FDH	R/W	00H	Flash Identification Register
FMCR	FEH	R/W	00H	Flash Mode Control Register

Register Map

12.1.2 REGISTER DESCRIPTION

FSADRH (Flash Sector Address High Register) : FAH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	FSADRH3	FSADRH2	FSADRH1	FSADRH0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

FSADRH[7:0] Flash Sector Address High

FSADRM (Flash Sector Address Middle Register) : FBH

.7	.6	.5	.4	.3	.2	.1	.0
FSADRM7	FSADRM6	FSADRM5	FSADRM4	FSADRM3	FSADRM2	FSADRM1	FSADRM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FSADRM[7:0] Flash Sector Address Middle

FSADRL (Flash Sector Address Low Register) : FCH

.7	.6	.5	.4	.3	.2	.1	.0
FSADRL7	FSADRL6	FSADRL5	FSADRL4	FSADRL3	FSADRL2	FSADRL1	FSADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FSADRL[7:0] Flash Sector Address Low

FIDR (Flash Identification Register) : FDH

.7	.6	.5	.4	.3	.2	.1	.0
FIDR7	FIDR6	FIDR5	FIDR4	FIDR3	FIDR2	FIDR1	FIDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FIDR[7:0] Flash Identification

Others No identification value

10100101 Identification value for a flash mode

(These bits are automatically cleared to logic ‘00H’ immediately after one time operation except “flash page buffer reset mode”)

FMCR (Flash Mode Control Register) : FEH

.7	.6	.5	.4	.3	.2	.1	.0
FMBUSY	–	–	–	–	FMCR2	FMCR1	FMCR0
R	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

FMBUSY Flash mode busy bit. This bit will be used for only debugger.

0 No effect when “1” is written

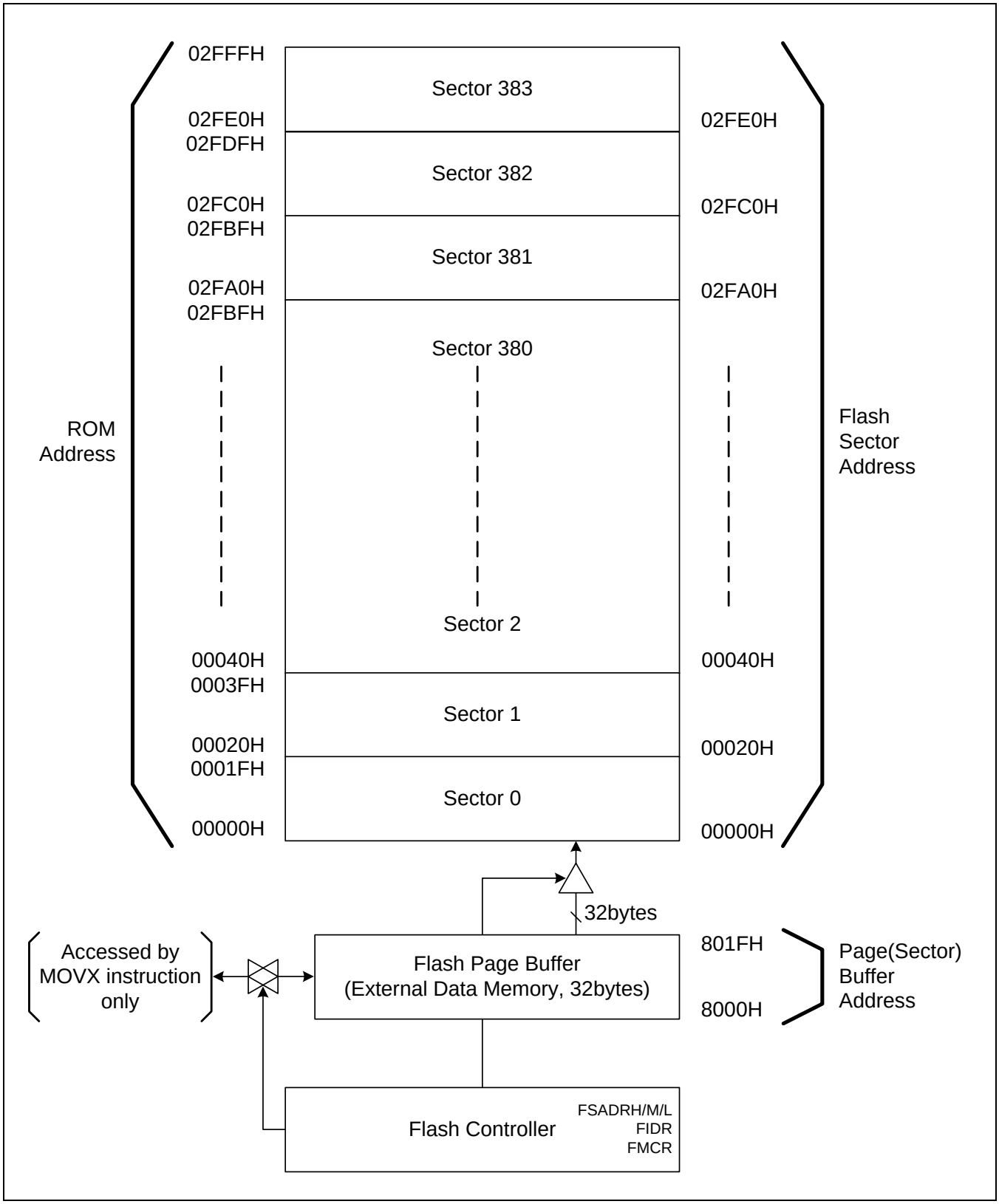
1 Busy

FMCR[2:0] Flash Mode Control Bits. During a flash mode operation, the CPU is hold and the global interrupt is on disable state regardless of the IE.7 (EA) bit.

FMCR2	FMCR1	FMCR	Description
0	0	1	Select flash page buffer reset mode and start regardless of the FIDR value (Clear all 32bytes to ‘0’)
0	1	0	Select flash sector erase mode and start operation when the FIDR=”10100101b”
0	1	1	Select flash sector write mode and start operation when the FIDR=”10100101b”
1	0	0	Select flash hard-lock mode and start operation when the FIDR=”10100101b”

Other Values: No operation
(These bits are automatically cleared to logic ‘00H’ immediately after one time operation)

12.2 FLASH PROGRAM ROM STRUCTURE



13. CONFIGURE OPTION

13.1 CONFIGURE OPTION

CONFIGURE OPTION 1 : ROM Address 001EH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN Enable Specific Area Write Protection

0 Disable Protection (Erasable by instruction)

1 Enable Protection (Not erasable by instruction)

PASS[2:0] Select Specific Area for Write Protection

NOTE) When PAEN = '1', it is applied

PASS2	PASS1	PASSS0	description
0	0	0	0.7K Bytes (0100h – 03FFH)
0	0	1	1.7K Bytes (0100h – 07FFH)
0	1	0	2.7K Bytes (0100h – 0BFFH)
0	1	1	3.7K Bytes (0100h – 0FFFH)
1	0	0	9.7K Bytes (0100h – 27FFH)
1	0	1	10.7K Bytes (0100h – 2BFFH)
1	1	0	11.2K Bytes (0100h – 2DFFH)
1	1	1	11.5K Bytes (0100h – 2EFFH)

CONFIGURE OPTION 2 : ROM Address 001FH

.7	.6	.5	.4	.3	.2	.1	.0
R_P	HL	–	VAPEN	–	FBS	–	RSTS

Initial value: 00H

R_P Code Read Protection

0 Disable

1 Enable

HL Code Write Protection

0 Disable

1 Enable

VAPEN Vector Area (00H – FFH) Protection Enable/Disable

0 Disable Protection (Erasable by instruction)

1 Enable Protection (Not erasable by instruction)

FBS OSC feedback resistor (RX1) Select

0 2400kΩ (VDD = 3V)

1 1000kΩ (VDD = 3V)

RSTS Select RESETB pin

0 Disable RESETB pin (P42)

1 Enable RESETB pin with a pull-up resistor

14. 설계 시 유의사항

1. 오타 및 탈자 발견하면 연락주세요.
2. 불명확한 부분 발견하면 연락주세요.

15. REVIEW HISTORY

Rev. No.	변 경 전	변 경 후	수정된 페이지
0.1	1. LCD duty: up to 1/4duty	1. LCD duty: up to 1/5duty (어보브 요청, 오명규수석)	다수 페이지
0.3	-	1. Added ADC, LCD 8COM, IAMP	다수 페이지
0.4	-	1. Added IRC s/w trim	18,33,35,38,69,74
0.5	-	1. Changed LCD bias figure 2. Changed Invertor Amp Enable bits 3. Changed Pin Name: VLC0 ← VLC1 4. Added main osc feedback resistor option	113, 114 120, 121 6,7,9,10,20,58 21,135
0.6	1. Inverter Amp	1. Changed inverter amp pin assign order	6-10,51,52
1.0	1. Vop: 1.8V to 5.5V 2. ADC: -	1. 1.8V to 3.6V 2. ADC: Added V_{BGR} input	다수 페이지 ADC Part
1.1	-	1. Removed LCD Bias 2R resistor	109,113,114
1.2	1. LFIRC: +/- 5% 2. VBGR: 0.91V 3. LCD BL: 15/25/35 mA 4. Flash Er: 2.5ms	1. LFIRC: +/- 10% 2. VBGR: 1.21V 3. LCD BL Current: 10/20/30 mA 4. Flash Er: 3.0ms, Added pre-program	다수페이지
1.3	1. - 2. -	1. Added Inverter Amp DC characteristics 2. Detail figure for inverter amp	21 120
1.4	-	1. Removed x-tal filter selection register	Related page
1.5	1. 48TQFP	1. Changed 48LQFP	4,7